D5.3. Analysis of results of the switching tests of the converters

Reinventing High-performance pOwer converters for heavy-Duty electric trAnSport

Grant Agreement Number 101056896

Deliverable name:	Analysis of results of the switching tests of the converters
Deliverable number:	5.3
Deliverable type:	R
Work Package:	WP5: Integration, testing and technical and environmental validation
Lead beneficiary:	Austrian Institute of Technology
Contact person:	Bernd Plassnegger; Bernd.Plassnegger@ait.ac.at Laura Hilscher; Laura.Hilscher@ait.ac.at
Dissemination Level:	PU
Due date for deliverable:	July 31, 2025

Funded by the European Union

Funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or CINEA. Neither the European Union nor the granting authority can be held responsible for them.

DOCUMENT CONTROL PAGE

Author(s):	Bernd Plassnegger, Laura Hilscher
Contributor(s):	Markus Koller, David Lumbreras
Reviewer(s):	Pawel Wojtal, Rafal Sala and Akash Kadechkar
Version number:	v.11
Contractual delivery date:	31 - 07 - 2025
Actual delivery date:	22 - 12 - 2025
Status:	Submitted

REVISION HISTORY

Version	Date	Author/Reviewer	Notes
v.0	12 – 03 – 2025	Markus Koller	Creation, First Draft
v.1	21 – 03 – 2025	Bernd Plassnegger	Chapter 2 and 3
v.2	22 – 04 – 2025	Pawel Wojtal & Rafal Sala	Deliverable Review/Revise
v.3	25 – 04 – 2025	Bernd Plassnegger & Markus Koller	Implementation of corrections
v.4	15 – 09 – 2025	Laura Hilscher	Second Design- Driver design and key objectives
v.5	16 – 10 – 2025	Markus Koller	Review
v.6	27 – 11 – 2025	Nestor Berbel & Markus Koller	Added chapter 4
v.7	01 – 12 – 2025	David Lumbreras	Format corrections applied and List of Acronyms completed. Updates to Section 1.1, Executive Summary, Section 4, and Conclusions. Hardware subsection removed.
v.8	09 – 12 – 2025	Pawel Wojtal & Rafal Sala	Deliverable Review
v.9	11 – 12 – 2025	Akash Kadechkar	Deliverable Review
v.10	18 – 12 – 2025	Peter Scheuermann	Implementation of corrections
v.11	22 – 12 – 2025	Luis Romeral	Submitted

ACKNOWLEDGEMENTS

The work described in this publication was subsidised by Horizon Europe (HORIZON) framework through the Grant Agreement Number 101056896.

DISCLAIMER

TABLE OF CONTENTS

EXECUTIVE SUMMARY

This deliverable reports on the switching tests validating the driver design of the high-power 150 kW hybrid T-Type converter for the RHODaS project. The study addresses the challenges of integrating Wide Band Gap (WBG) semiconductors, specifically Gallium Nitride (GaN) and Silicon Carbide (SiC), in high-voltage configurations to enhance efficiency. While the initial prototype faced reliability issues, a redesign utilising GaN Systems devices (GS66516B) and negative turn-off voltage successfully mitigated parasitic turn-on risks.

Experimental analysis confirmed robust operation up to 1000 V. However, high commutation loop inductance (≈100 nH) necessitated limiting switching rise times to 70–100 ns via adjusted gate parameters (R_{gate}=22 Ω, C_{gate}=4.7 nF). This adjustment prioritised reliability over minimal switching losses. Regarding control, whilst advanced CBPWM and SPWM strategies were implemented in the System on Chip (SoC), some constraints prevented their full experimental validation. Thus, standard Space Vector Modulation (SVPWM) will be employed for final testing.

In conclusion, the project delivered a robust GaN stage capable of 1000 V operation, though the validation of custom modulation techniques remains pending.

LIST OF ACCRONYMS

Acronyms	Definition
AIT	Austrian Institute of Technology
AXI	Advanced eXtensible Interface
CB-PWM	Carrier-Based Pulse Width Modulation
DC	Direct Current
DPT	Double Pulse Tests
FPGA	Field-Programmable Gate Array
GaN	Gallium Nitride
GND	Ground
ILA	Integrated Logic Analyzer
PCB	Printed Circuit Board
PWM	Pulse-width modulation
RHODAS	Reinventing High-performance pOwer converters for heavy-Duty electric trAnSport
SiC	Silicon Carbide
SoC	System on a Chip
SPWM	Sinusoidal Pulse Width Modulation
SVM	Space Vector Modulation
SVPWM	Space Vector Pulse Width Modulation
TIM	Thermal Interface Material
UPC	Universitat Politècnica de Catalunya

1 INTRODUCTION

1.1 DESCRIPTION OF THE DOCUMENT AND PURSUE

This report describes the RHODAS project's efforts within Work Package 5, focusing specifically on Task 5.4, which covers the analysis and validation of the switching performance of the hybrid T-Type converter's GaN power stage. The document details the results of two distinct development iterations of the GaN power stage: the initial design, which utilised pre-series Infineon GaNs with integrated drivers and ultimately failed, and the subsequent, successfully validated iteration, utilising the reliable GaN Systems transistors with external drivers. This analysis demonstrates the robustness, high-voltage capability (up to 1000 V DC link), and fault mitigation necessary for the heavy-duty application.

The report also includes information on the simulation and implementation of advanced control modulation strategies, namely Carrier-Based Pulse Width Modulation (CB-PWM) for three-level operation and Sinusoidal Pulse Width Modulation (SVPWM) for two-level operation. These strategies were prepared as an IP block for the System on a Chip (SoC) control platform. The final validation with the high-power inverter was performed by simulation.

1.2 WPS AND TASKS RELATED WITH THE DELIVERABLE

This deliverable refers to Task 5.4 included in WP5: Integration, testing and technical and environmental validation.

2 FIRST DESIGN

After the PCB design, the configuration and adjustment of the switching behaviour through the gate driver is a critical process.

The main objectives of the PCB layout were:

- **Minimizing stray inductances in the bridge**. This is intended to enable fast switching. However, it should be noted that achieving extremely fast switching to fully exploit the potential of the GaNs is not possible in this design. The parallelization itself introduces a significantly large loop, which inherently limits the switching speed.
- **Optimizing current paths and preventing mutual influence between the load current and voltage and the gate drive**. This requirement was fulfilled as much as possible. The load currents paths are designed to be always close to 90° relative to the driver paths. The gate traces of the integrated drivers are routed directly over the GaN with isolated GND in between, and the vias are placed as close together as possible to minimize loop areas between the forward and return paths. However, via connections are inherently not ideal, as they introduce high inductances. In this case, avoiding them entirely was not feasible.

Now in the driver design, the focus is on:

- **Avoiding over voltages.** The switching speed is the critical factor in this design. It must be carefully selected to prevent critical conditions that could damage the GaN devices.
- **Avoiding parasitic turn-on to prevent short circuits and unintended switching events**. Verification through measurements under critical conditions to ensure that no unintended turn-on occurs.

2.1 SWITCHING SPEED AND DRIVER VOLTAGE

Since the drivers themselves cannot use a permanent negative supply voltage, the negative gate drive voltage builds up at the beginning of the switching process. The design is shown in Figure 1, where a time constant of approximately 470 µs was chosen.

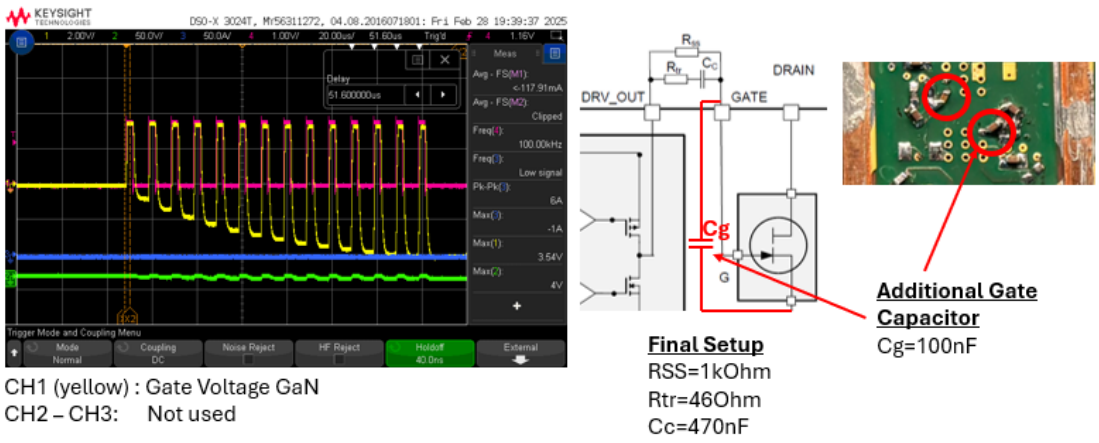
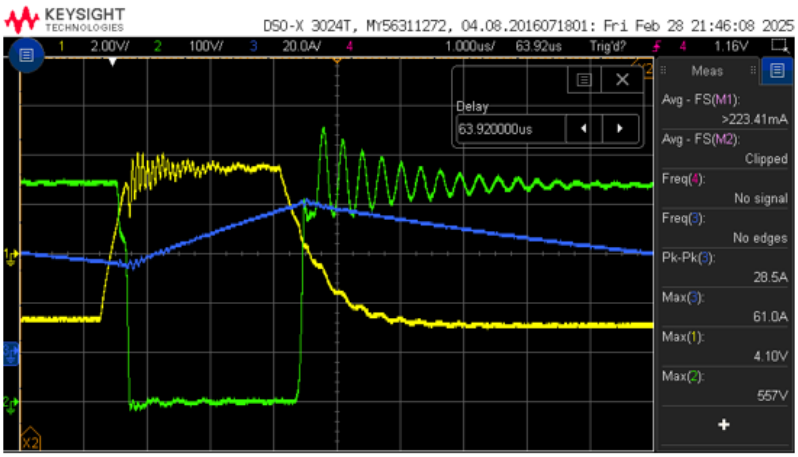


Figure 1. Build-up of the Negative Gate Drive Voltage (left) and Final Driver Circuit (right).

Figure 1 also provides a measurement with a very high switching frequency of 100 kHz. The key takeaway for our application is that the GaNs must always switch in 2-level

operation to ensure that a negative gate voltage is consistently available. In 2-level operation, each GaN device undergoes a full switching transition during every switching cycle, ensuring regular and sufficiently large dv/dt and di/dt events at the switching node. These transitions consistently drive the gate-drive coupling network (e.g., via Cg and the Miller path), allowing the negative gate voltage to be reliably regenerated each cycle, even at high switching frequencies such as 100 kHz. In contrast, multi-level or partial-level operation reduces or eliminates full voltage swings across the device, which can prevent adequate charge transfer and lead to an insufficient or unstable negative gate bias. Therefore, strict 2-level operation is required to guarantee a consistently available negative gate voltage for safe and robust GaN turn-off behavior.

The switching speed aim is less than 100 ns**,** which is below the maximum capability of the GaN devices but represents a realistic and practical target. Also shows that an additional 100 nF capacitor was directly soldered to the gate to slow down the switching speed. Figure 2 shows a switching test with an inductive load. The gate voltage is also measured directly at the gate without clamps to ensure that any problems on the gate during switching with 800 VDC link can be seen.



CH1 (Yellow) : Gate Voltage at switched GaN
CH2 (Green) : Voltage over GaN Stage (2 GaNs in Series)
CH3 (Blue) : Output current (Inductive Load)

Ch(1) Gate voltage directly measured on GaN gate without clamps.

Figure 2. GaN Switching Speed Measurement for 800 VDC.

Figure 3 shows turn-on and turn-off in detail, allowing the switching speeds to be more clearly observed from the waveform.

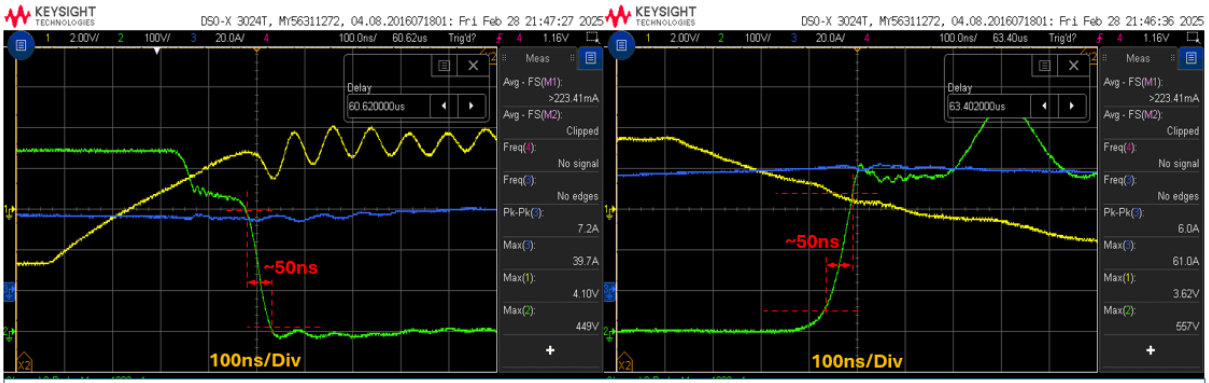


Figure 3. GaN Switching Speed Measurement for 800 VDC in Detail.

Switching takes about 50 ns for both turn-on and turn-off. It should be noted that the voltage was measured across both GaNs to avoid capturing potential shifts between the two antiparallel-connected devices. Thus, the measurement also includes the voltage across the GaN that is conducting passively, as well as the voltage across the parasitic inductance of the GaN branch. The result reflects therefore the output voltage of the half-bridge and represents the voltage present at the inverter output.

2.2 OVERVOLTAGE SWITCHING TEST

For this test, the voltage was measured directly at a switching GaN at 194 A, both at the gate and across the switching device, using direct probing without clamps. The goal was to determine whether dangerous over voltages occur during operation.

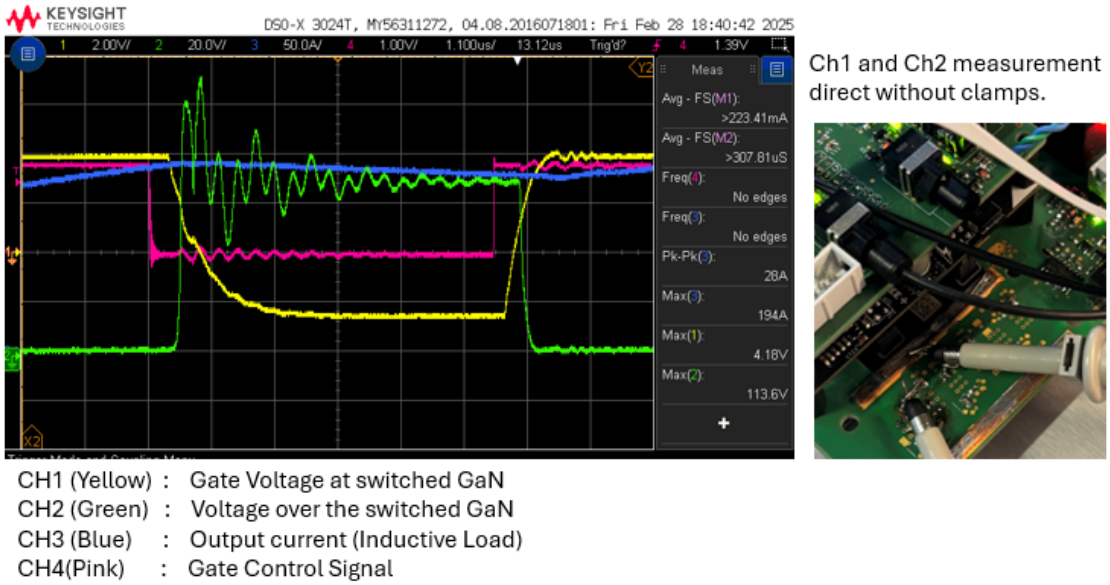


Figure 4. GaN Switching-Off Test with 194 A.

This test was conducted with a DC link voltage of approximately 80 V. The voltage overshoot depends on the current, and therefore the results can also be applied to higher DC link voltages.

A second switching test with 405 A was also carried out before commissioning, following the initial tests which are shown in Figure 5.

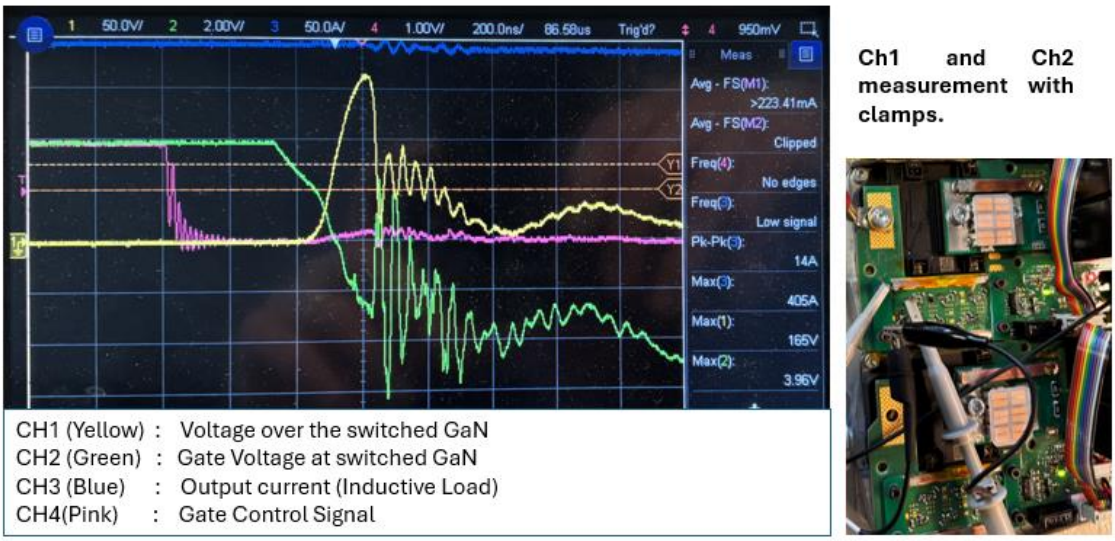


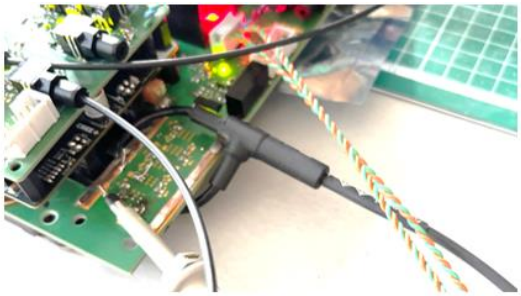
Figure 5. GaN Switching-Off Test with 400 A.

However, this measurement is only available as an image and was performed using clamp probes. The reason is that this measurement was done to verify the functionality before performing clean measurements. Unfortunately, the clean measurements without clamps were not saved, that was noticed after the inverter was already destroyed. The inverter had been mounted on the test bench and put into operation without delay immediately after these measurements. Nevertheless, it can be concluded that during turn-off at 400 A, an overvoltage of around 160 V occurred, which is consistent with the earlier measurement.

The strong high-frequency oscillations visible at the gate in this case are not actually present; they influence from the use of clamp probes. At a resolution of 2 V/div, their influence on the gate signal is significantly greater than on the overvoltage measurement at the GaN.

2.3 PARASITIC TURN ON TEST

A concern was that due to lack of negative gate voltage the GaNs could turn on parasitic while the SiCs start switching. This is only curtailed at the first turn on, because of the built-in driver of the GaNs. This test was also done with both GaNs turned off the whole test and just started switching the SiCs Bride at a DC Link Voltage of 800 VDC. Figure 6 shows the result of this test.



SiC switching setup, also with a Rogowski coil setup to measure parasitic turn-on of the GaNs without negative gate voltage on the GaN driver.

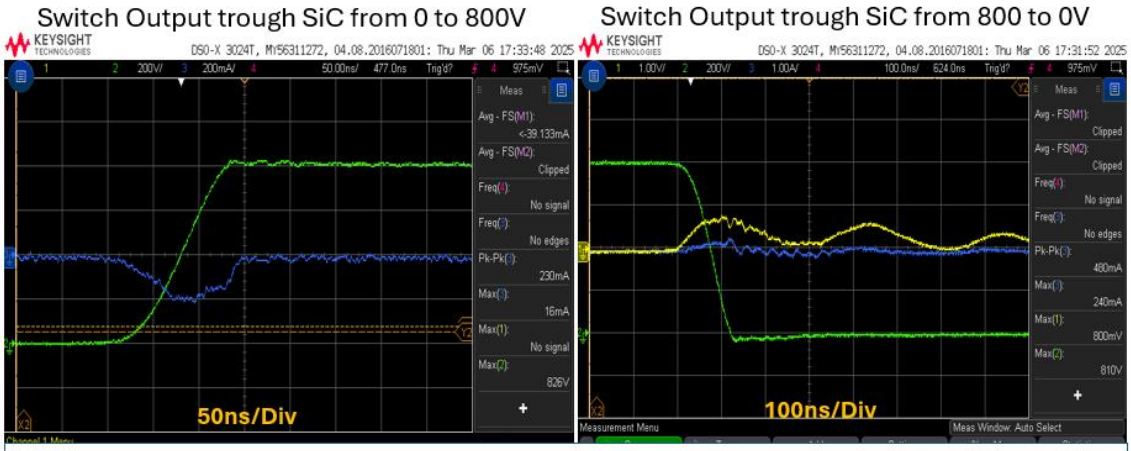


Figure 6. GaN Parasitic Turn-On Test.

In the left measurement, the gate voltage is turned off, and the current scaling is different. There is no parasitic turn-on, although the gate voltage sees some ringing. The observed current appears to result mainly from the redistribution of charge in the parasitic capacitance of the GaNs and the GaN stage.

It is also worth mentioning that the switching speed of the SiCs was intentionally limited so that they do not switch faster than the GaNs. As a result of this reduction, the turn-on and turn-off times are approximately 70–80 ns. This measure is intended to minimize interference with the GaN drivers and to avoid over voltages.

2.4 CONSEQUENCES

Adjusting the GaNs with integrated drivers proved to be quite complex, as each modification had to be followed by thorough testing. The results of the switching tests were generally promising, although it was always clear that working with pre series GaNs involves a high risk of failure. GaN devices in general are inherently sensitive, especially when operated at 800 V and in half-bridge configurations. To ensure safe long-term operation, an external robust driver circuit with reliable GaNs are necessary. Also, additional GaN protection circuit as a desaturation detection would be advantageous. Such a solution is currently not feasible, as the required response time, from detection to shut down, would need to be around 100 ns, which is not reliably achievable today.

After the first design failed at inverter operation due to the unreliable GaN stage and no further GaNs by Infineon were available anymore, a new and more reliable GaN power stage was designed.

Nevertheless, it was demonstrated that switching was generally possible, and the topology could work with some design changes and adjustments for a new design.

3 SECOND DESIGN

The main objectives for the redesign remained the same as for the first design:

- **Minimizing stray inductances in the bridge**. The design focused as the first design on minimizing stray inductances. Since SiC modules were used in combination with substituted discrete GaN semiconductors a certain distance of the semiconductors was unavoidable. The original component placement also had to be retained so that heat sinks, housings, and other circuit boards could be retained. This resulted in restrictions on the placement of components, and the commutation loops could not be made shorter. Therefore, extremely fast switching to fully exploit the potential of the GaNs was not possible in this design.
- **Avoiding over-voltages.** The switching speed was the critical factor in the design. It must be carefully selected to prevent critical conditions, especially over voltages. Since the converter should be operated at 1000 V the switching speed was limited to below 100 ns to protect GaN devices from damage trough overvoltage.
- **Avoiding parasitic turn-on to prevent short circuits and unintended switching events**. This objective was critical for the new design. To make sure, that no parasitic turn-on would be possible the new GaNs were switched with a negative turn off voltage.

3.1 REDESIGN OF THE GAN STAGE

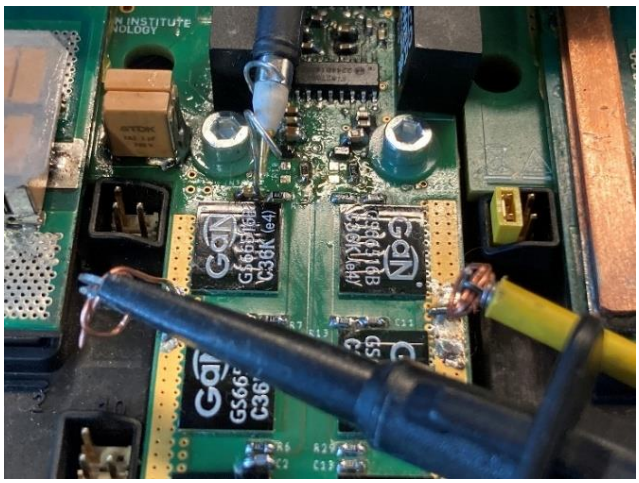
The first inverter was destroyed due to the unreliable GaN stage. Therefore, the inverter and especially the GaN stage had to be repaired and rebuilt. Unfortunately, the used GaNs with the integrated power stage were early prototypes and they were discontinued by Infineon. This meant that they were not even available anymore since production had stopped.

Therefore, a completely new GaN stage had to be designed with different GaNs. Due to the complexity of the system this meant that a completely new power stage had to be designed and fitted on to the existing heatsink and into the housing, not only with the GaNs and drivers but also the DC-link capacitors.

The new design featured GaNs by GaN Systems (GS66516B) which were well approved semiconductors with drivers (SI8275BBD-IS1) that have been separately chosen.

The biggest advantage of the new design was that the GaNs have a negative turn off voltage that reduces the risk of a parasitic turn on. At the same time, some disadvantages had to be accepted. A negative turn off voltage also implies slightly higher losses while in dead time operation. In addition to that the Rdson of the GaNs Systems semiconductors were slightly higher (25 mΩ instead of 17 mΩ) than the CoolGaN.

3.2 DOUBLE PULSE TESTS



Double pulse tests were carried out to verify the functionality of one phase of the T-branch and to tune the gate capacitance and gate resistance into the required switching rise time.

The test setup was carried out in a way, that only one GaN had to be switched and the other GaN was permanently “ON”.

The commutation took place between the SiCs freewheeling Diode and the switched GaN using an inductive load.

Figure 7. Measurement setup of gate signals

shows the measurement setup with an oscilloscope 500 MHz passive probe on the gate and an active differential probe (TESTEC 100 MHz) across the two GaN semiconductors. The load current was measured with a Hioki current clamp. Since this test setup only used one SiC and one switched GaN over the half DC link voltage, 400 V was applied, which corresponds to the same operating conditions as would exist at 800 V in 3 level operation mode of one phase.

3.3 RISE TIME AND OVERVOLTAGES

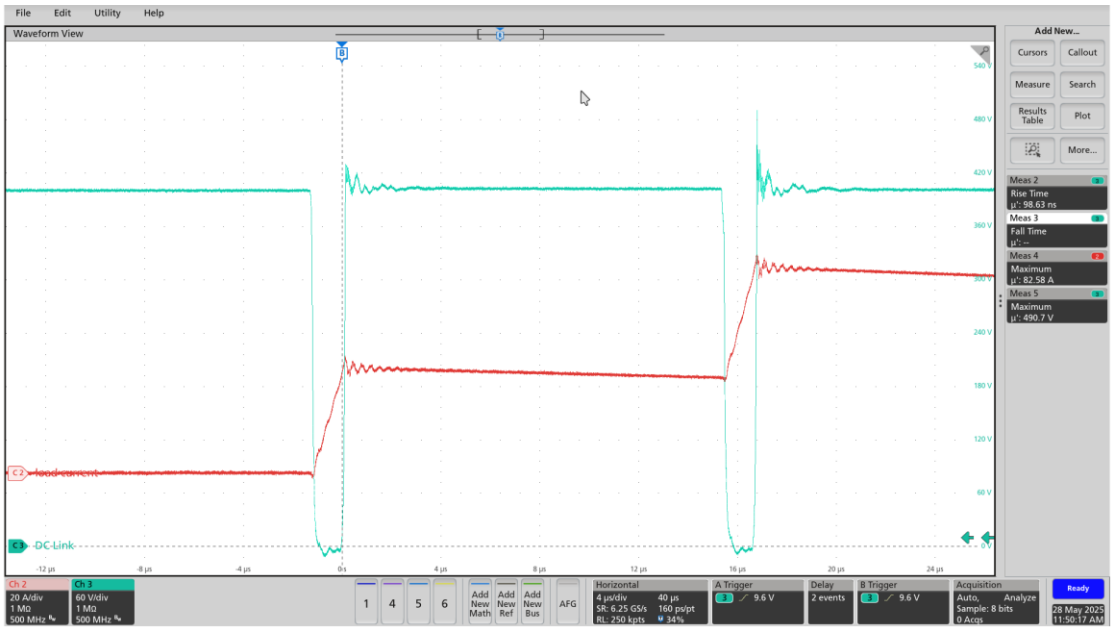


Figure 8. Double Pulse test with measured voltage across the GaNs (green) and the current trough the inductive load (red).

First, double pulse tests were performed at 400 V. It can be seen in Figure 8, that when the current (red) is built up there is a high voltage overshoot (green). To keep the voltage overshoot within certain limits the rise time of the voltage and therefore the rise time of the current, had to be slowed down into the range of 70-100 ns, even accepting higher losses in the semiconductors. The voltage overshoot corresponds to a parasitic

inductance of the commutation loop of around 100 nH between the SiC module and the GaNs.
Since SiC modules were used in combination with discrete GaN semiconductors a certain distance between the semiconductors was unavoidable, resulting in the relatively high parasitic inductance of the commutation loop.

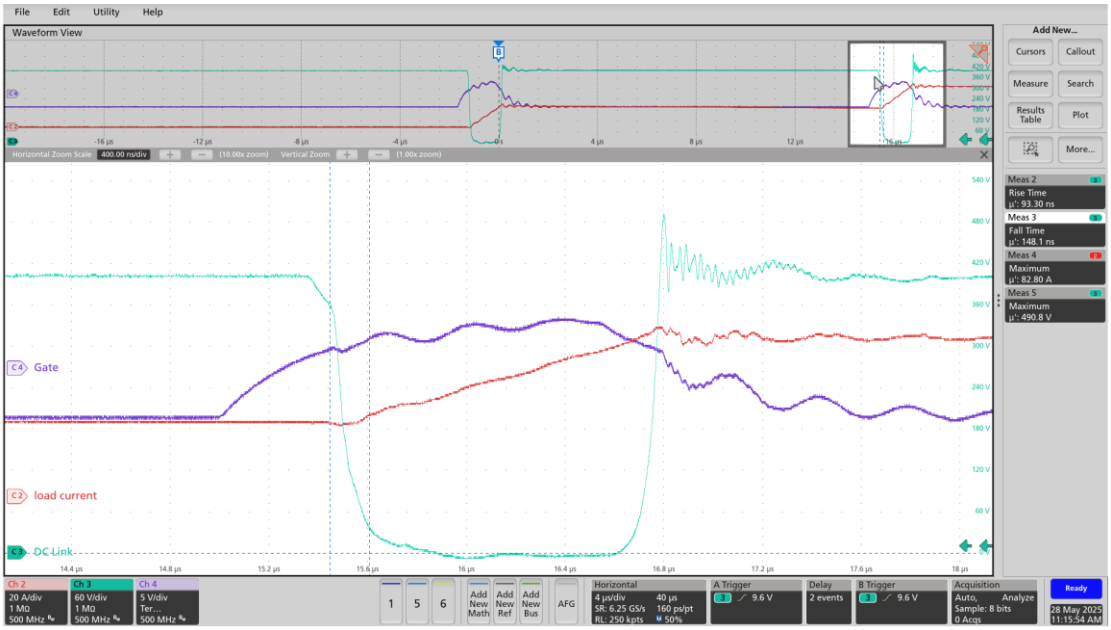


Figure 9. Zoomed in. Double pulse test with voltage (green), current (red), gate voltage (purple).

Figure 9 shows a switching action (green) with load current (red) and with gate voltage (purple). Although the gate voltage probe was connected as close as possible (as shown in) to the gate there is still some ringing visible. This is because there are some parasitic inductances at the gates, since three GaNs are in parallel. Also, the additional external gate capacitances unfortunately add parasitic inductances to the gate circuit. Altogether, this ringing has not much effect on the switching performance.

3.4 DOUBLE PULSE TESTS AT 500 V

After the double pulse tests the whole inverter was tested successfully at 800 V DC link voltage. Only after those measurements double pulse tests and endurance tests with a resistor and inductive load were performed at 500 V for one phase- corresponding to the 1000 V DC link in the final inverter.

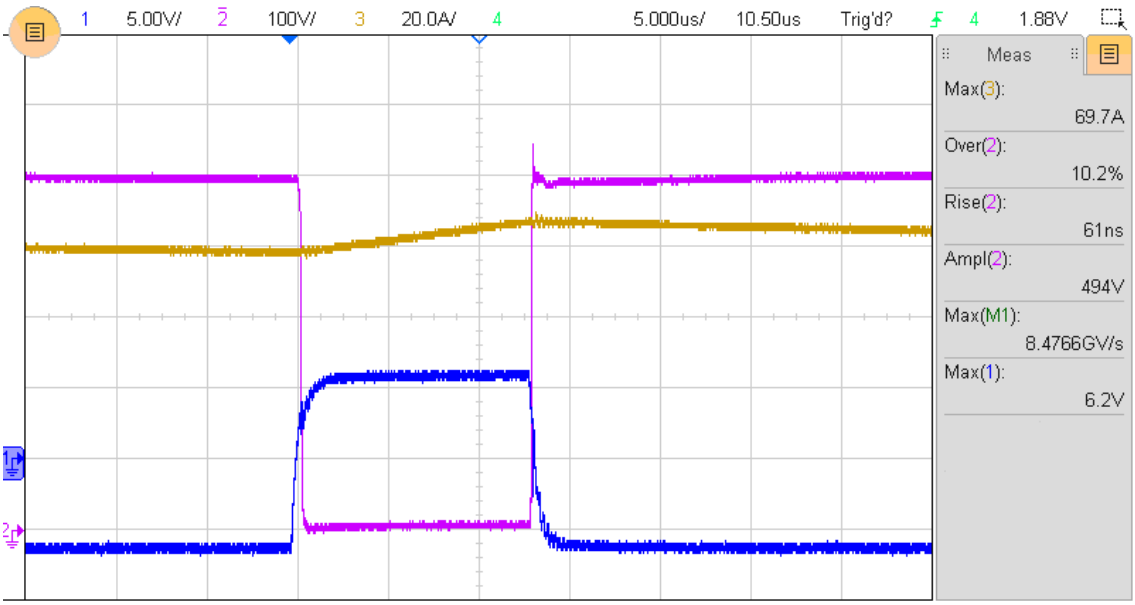


Figure 10. Tests at 500V-correspondig to 1000V DC Link; voltage across GaNs (purple), load current (brown), gate voltage (blue).

The measurements showed good results, hinting, that the inverter was capable of 1000 V DC link. The oscilloscopes probes were connected to well accessible positions at the power stage. This was done to avoid soldering extra pins on a fragile part of the gate. At 500 V on the GaN semiconductors the measurements only showed a voltage overshoot of around 10.2 % (see **Figure 12)**, which is 50 V in this case and surprisingly good. Unfortunately, the probe for the voltage across the GaNs was also positioned relatively far away from the GaNs, but on a well accessible place, reducing the visibility of voltage overshoot. It can be assumed, that the real voltage overshoot was not only 50 V, but around 100 V, corresponding to the primarily calculated ~100 nH parasitic inductance of the commutation loop circuit. Nevertheless, the GaNs by GaN Systems are rated to a Drain-to-Source voltage of 650 V, which means that there is enough safety margin, as long as the load current stays below ~90 A. Transiently the GaNs are rated even higher,

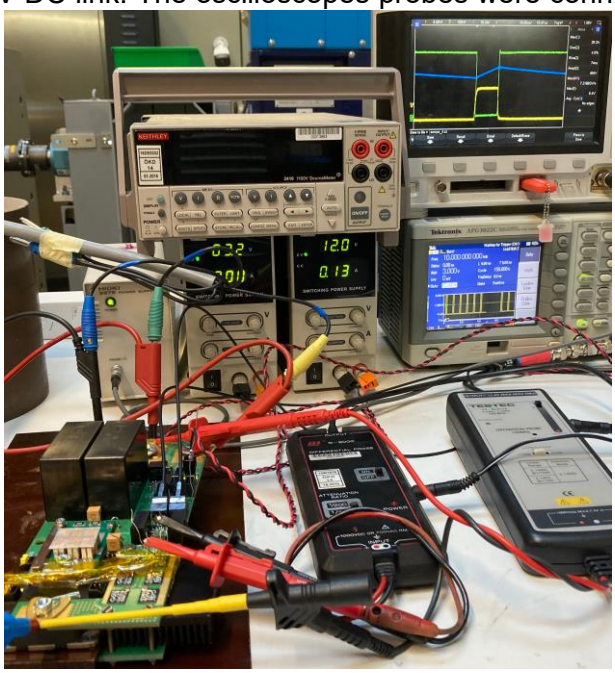


Figure 11. Experimental setup

surviving 750 V based on the datasheet, meaning, that the circuit will not break down at even more load current due to overvoltage.

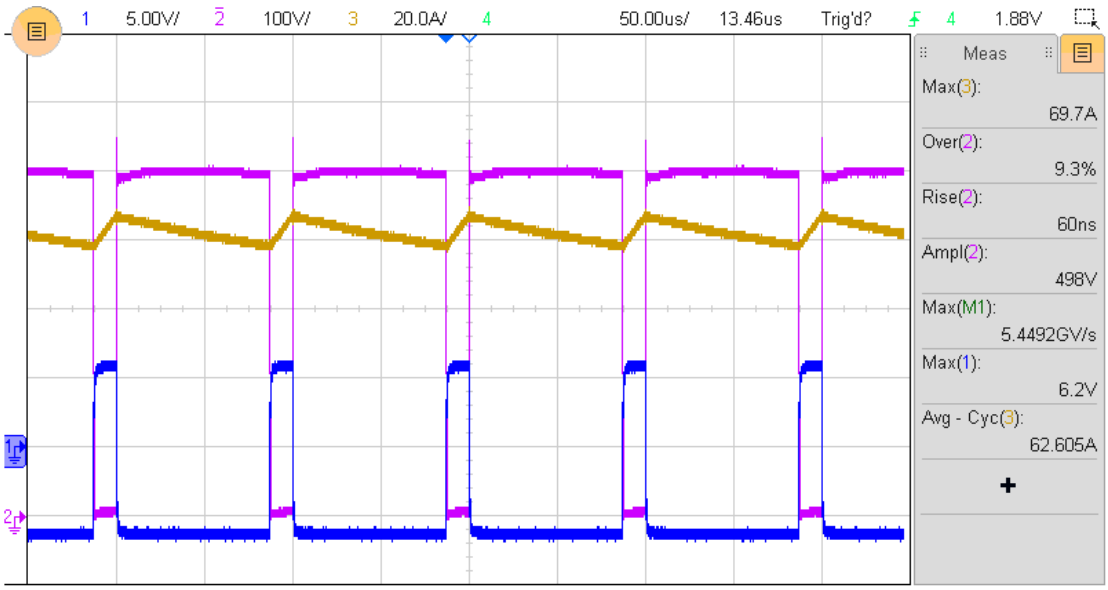


Figure 12. Endurance test at 500V.

Endurance tests were performed at 500 V with a resistor and inductor, as shown in Figure 12. No problems occurred, so tests could be performed at 1000 V on the inverter.

3.5 SWITCHING BEHAVIOR IN INVERTER SETUP

The complete inverter was tested at 800 V up to 1000 V in 2 level and in 3 level mode. Temperature measurements were performed with a thermal camera where videos were recorded. At a low output frequency (10 rpm) and an output current of around 30 A the temperature of the GaNs was visibly pulsating in the recording. Figure 15 shows pictures of the thermal camera as well as a photograph of the inverter for comparison. The temperature distribution between the paralleled GaNs look evenly distributed and it can be concluded that they are equally connected to the heatsink.

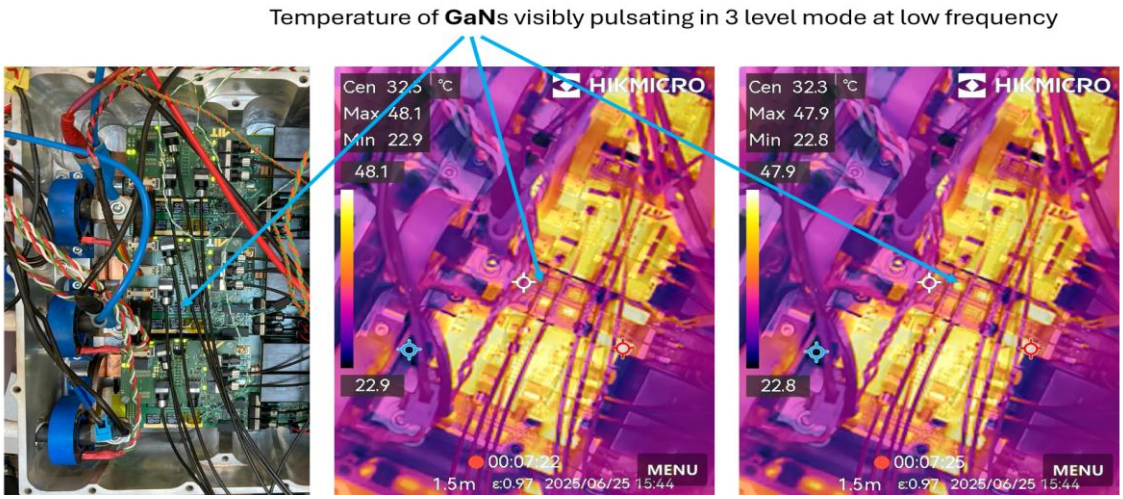


Figure 13. Foto of inverter(left); Thermal camera recording (right), where temperature of GaNs is visibly pulsating in 3 level mode

The phase to phase voltage measurements of the whole inverter were placed far away from the semicoductors therfore no useful voltage overshoot was visible. In inverter mode, the focus of the measurements was on correct voltage and current waveforms, rather than on individual voltage pulses. In Figure 14 the transition between 2 level mode and 3 level mode at 800 V DC link is shown as an example. The difference in 2 level and 3 level mode can be clearly seen. As expected, there are fewer harmonics in the current and voltage in 3-level mode.

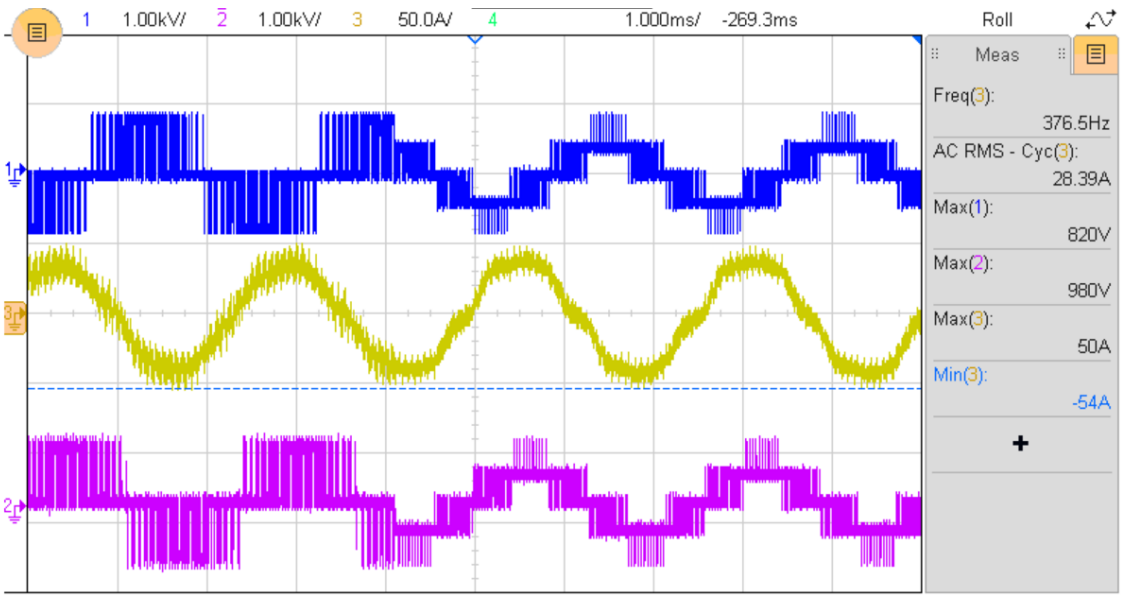


Figure 14. Transition from 2 level mode into 3 level mode, at 800V; Phase to phase voltage (blue, magenta), phase current (yellow)

4 SIMULATION OF ADVANCED PWM MODULATIONS

This section details the final switching patterns of the inverter, covering the simulation, implementation and current experimental status of the advanced modulation strategies developed for the high-power converter.

The power converter employs two modulation techniques:

- Carrier-Based Pulse Width Modulation (CB-PWM): Utilised for three-level operation (−VDC/2, 0V, or +VDC/2).
- Sinusoidal Pulse Width Modulation (SPWM): Utilised for two-level operation (−VDC/2 or +VDC/2).

These strategies were originally developed by UPC for the low-power converter prototype within WP2. Supporting simulation results were detailed in Deliverable D2.3, whilst experimental validation was presented in Deliverable D2.4. Consequently, the strategies implemented herein are identical to those previously verified at the low-power converter.

4.1 SIMULATION AND DIGITAL IMPLEMENTATION

To transfer the control strategies to the high-power prototype, simulations were performed by UPC using a co-simulation environment comprising MATLAB/Simulink and

Xilinx VHDL blocks. The converter topology was modelled within the SimPowerSystems toolbox, incorporating specific GaN and SiC MOSFET characteristics.

Table 1 details the parameters employed during the simulation. Figure 15 shows the simulation model.

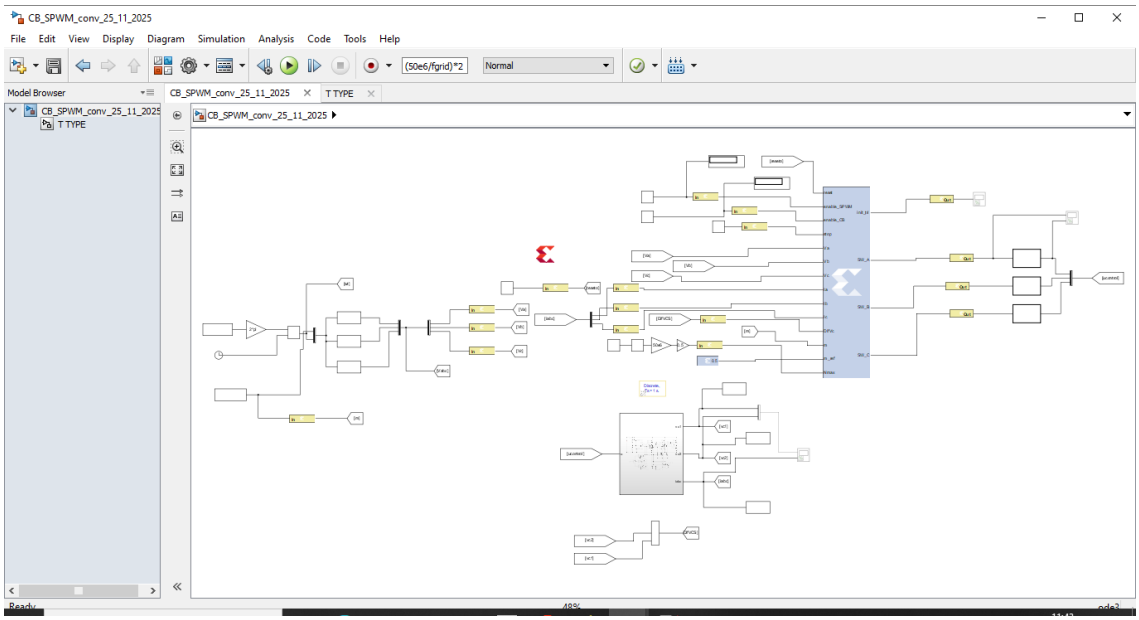


Figure 15. Simulation model in MATLAB Simulink.

Signal name	Value
f_{sw}	100 kHz
V_{DC}	800 V
$Modulation\ index$	0.75

Table 1. Simulation parameters.

Figure 16, Figure 17, and Figure 18, Y, and Z present the simulation results obtained during three-level operation, utilising the CB-PWM technique.

Figure 16 depicts the phase-to-neutral output voltage. This waveform exhibits three distinct levels ($+V_{DC}$, 0, and $-V_{DC}$), corresponding to the output states of the converter. To minimise abrupt voltage transitions (dv/dt), ringing, and switching losses, the commutation sequence is limited to transitions between adjacent levels (i.e., $+V_{DC} \leftrightarrow 0$ and $0 \leftrightarrow -V_{DC}$).

Figure 17 illustrates the phase-to-phase voltage. Whilst this waveform approximates a sinusoid, the stepped transitions arising from the discrete phase voltage levels remain observable. It is essential to note that these simulation results align precisely with the experimental results of the low-power converter previously reported in Deliverable D2.4.

Finally, Figure 18 displays the system currents. These waveforms are purely sinusoidal, except for a minor initial transient caused by the initialisation of simulation parameters.

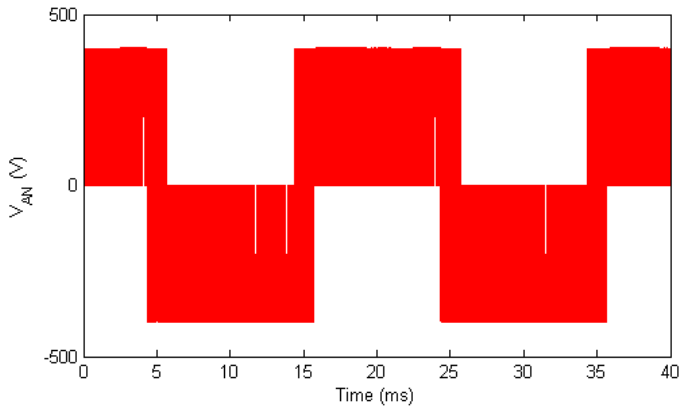


Figure 16. CB-PWM: Phase to neutral voltage.

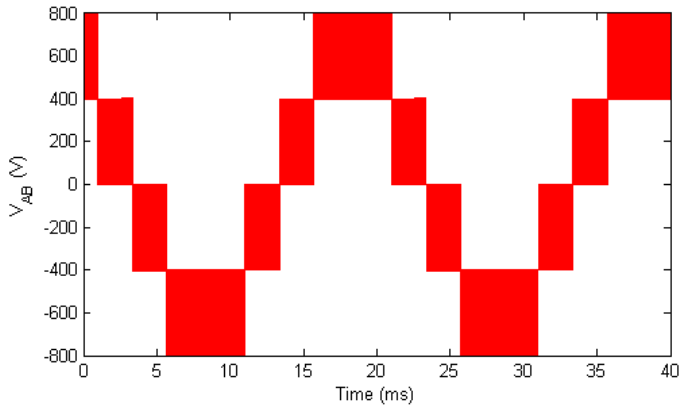


Figure 17. CB-PWM: Phase to phase voltage.

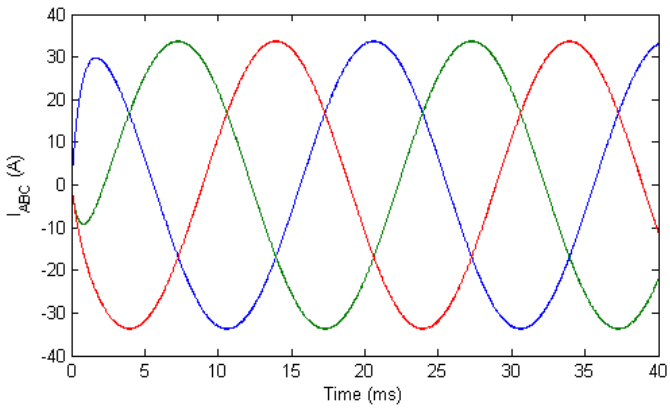


Figure 18. CB-PWM: Output current.

Figure 19, and Figure 20 present the results obtained during two-level operation, employing the SPWM technique.

Figure 19 shows the phase-to-phase output voltage, which toggles between two levels (+VDC and −VDC). This waveform exhibits a less sinusoidal profile compared to the three-level operation shown in Figure 17, as the converter modulates only two voltage levels at the output. Consequently, this operation mode yields a higher Total Harmonic Distortion. These results are also identical to the experimental validation presented in Deliverable D2.4.

Finally, Figure 20 depicts the system currents, which appear as ideal sinusoids following a brief initial transient due to simulation start-up parameters.

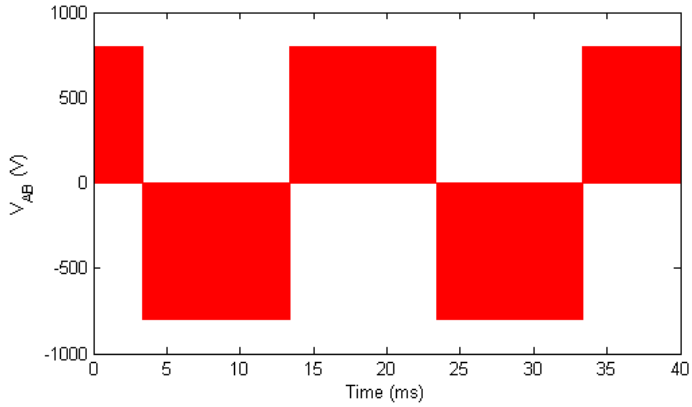


Figure 19. SPWM: Phase to phase voltage.

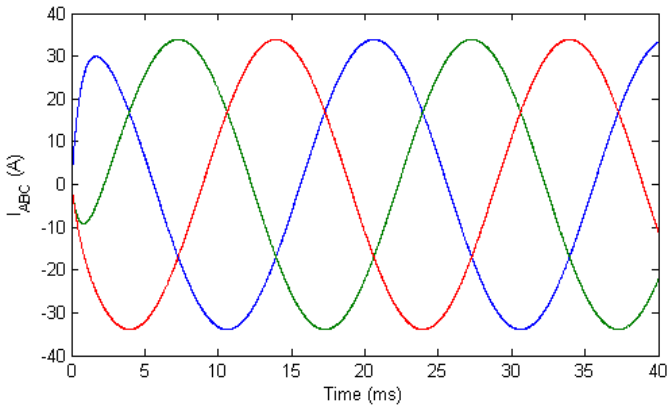


Figure 20. SPWM: Output current.

AIT implemented both modulation strategies as an IP block in the FPGA part of the system on a chip (Zynq-7000 SoC) which is used to control the high-power inverter. Figure 21 shows the IP block which is connected with the internal AXI bus.

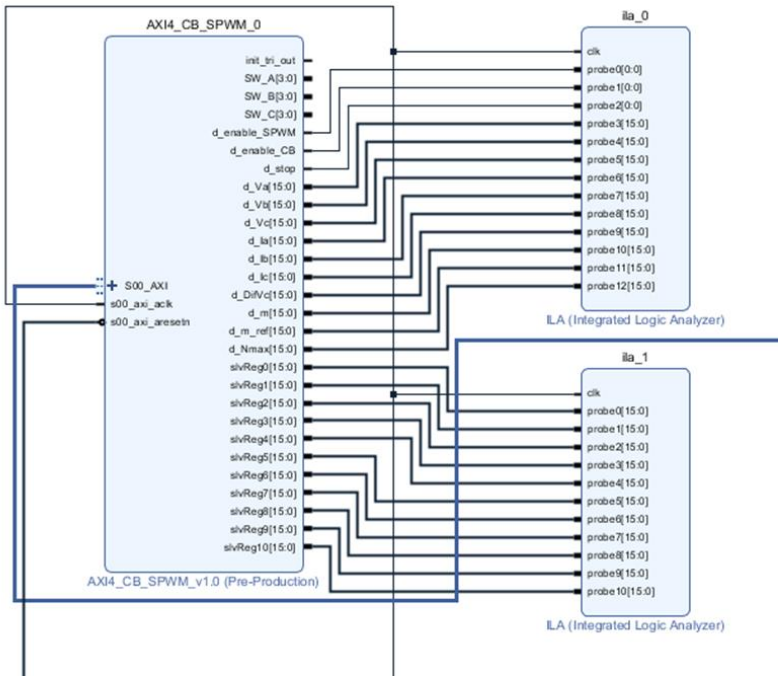


Figure 21. IP block of the proposed modulation.

The IP block was tested with the help of the integrated logic analyser. Figure 22 shows the waveform of the recorded output signals.

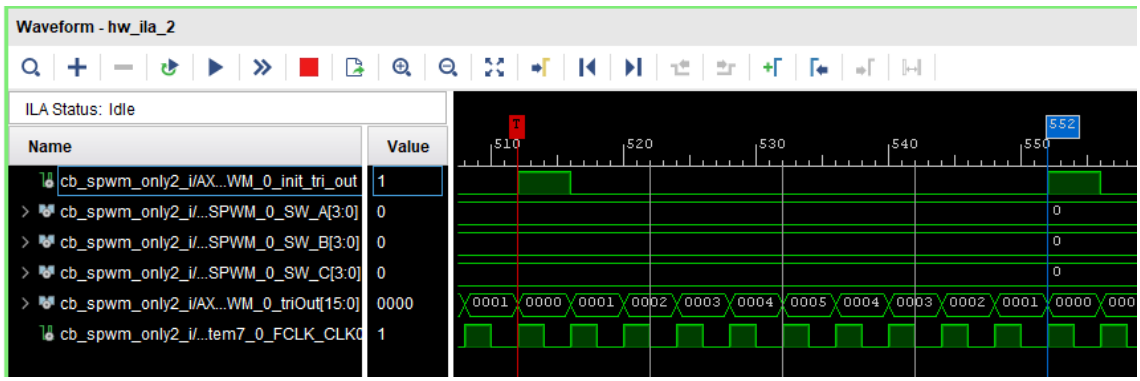


Figure 22. Waveform showing (Top down) the ADC trigger output, switching outputs, carrier signal and the internal clock.

4.2 VALIDATION STATUS

Validating the CB-PWM and SPWM strategies at the high-power converter is a mandatory requirement for this deliverable.

While the modulation IP blocks have been successfully implemented in the SoC hardware, the integrated IP block could not be validated on the high-power inverter test bench. To mitigate this, the high-voltage experiments (up to 1000 V), were conducted utilising an alternative Space Vector Pulse Width Modulation (SVPWM) strategy supplied by AIT. However, the two-level SPWM technique was validated and implemented in the high-power converter.

Consequently, the experimental verification of the custom switching patterns of the CB-PWM strategy remains pending. This represents a partial deviation from the objectives of Task 5.4.

5 CONCLUSION

This report presents the outcomes and analysis of the switching tests, focusing on the validation of the high-power hybrid T-Type converter.

The initial prototype, which incorporated SiC modules and pre-series Infineon CoolGaN devices, exhibited instability in a half-bridge configuration at high voltages. The failure was attributed to the absence of a negative gate drive capability in the pre-series devices, which led to their subsequent discontinuation by the manufacturer and the loss of the first inverter. Consequently, a robust redesign was implemented utilising commercial GaN Systems devices with independent drivers. This topology enables the application of a negative turn-off voltage, effectively mitigating the risk of parasitic turn-on. The redesign was successfully validated, demonstrating stable inverter operation at DC link voltages ranging from 800 V to 1000 V, thereby aligning with the project's high-voltage objectives.

The analysis confirmed that the parasitic inductance of the commutation loop (approximately 100 nH) imposes strict limits on the switching speed (dv/dt). To maintain voltage overshoots within the 750 V transient rating of the GaN devices, the rise time was intentionally constrained to the 70 ns – 100 ns range via increased gate resistance and capacitance. This design trade-off prioritised device protection over switching speed, resulting in slightly higher switching losses.

Regarding data acquisition, the accuracy of high-voltage measurements was influenced by technical constraints. Specifically, the true overvoltage during Double Pulse Tests at 500 V was partially obscured by probe placement limitations. Furthermore, data from the initial high-current tests (405 A) was compromised by the exclusive reliance on clamp probes before the inverter failure.

A deviation from TO1.3 and the full scope of Task 5.4 is noted regarding switching pattern validation. Whilst the advanced CB-PWM and SPWM modulation strategies were successfully developed, simulated, and instantiated as an IP block on the SoC FPGA, integration testing with the high-power inverter was not possible due to time constraints. However, high-power characterisation was performed using an alternative SVPWM technique, which allowed for the experimental verification of the high-power T-Type Power Inverter