D5.1. Description of the final prototype of the RHODaS hybrid T-Type power converter. Definition of scenarios and procedures for validation

Reinventing High-performance pOwer converters for heavy-Duty electric trAnSport

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TABLE OF CONTENTS

EXECUTIVE SUMMARY

This deliverable presents the design, validation, and testing of the RHODaS high-power hybrid T-type multilevel inverter. Chapter 2 explains the overall architecture of the inverter, including sensors, modular power stages, mechanical structure, housing, and integration. The first design of the power stage did not meet the electrical and thermal requirements; therefore, several improvements were introduced in the final stage, which are also described in this chapter. Both iterations, the initial and the final design, are documented to highlight the evolution of the system. Chapter 3 explains the initial T-type design and the challenges encountered with the first GaN transistors, such as voltage limitations, short-circuit behaviour, and reliability issues. Chapter 4 explains the initial inverter tests, including switching behaviour and operation at different load points, which were performed to ensure proper functionality. Finally, chapter 5 defines the comprehensive high-power inverter tests, covering efficiency, thermal performance, and maximum power capability, with final validation to be conducted at BOSMAL's mechanical testing laboratory.

In conclusion, the deliverable documents the progression from an initial design with critical shortcomings to a robust final inverter prototype, achieving a power density of 58.6 kW/l. The initial tests confirm that the converter is both reliable and capable of operating in line with the project specifications, reaching efficiencies of up to 99%. Nevertheless, the definitive validation of the converter will be conducted at BOSMAL, where the comprehensive test procedures defined in this deliverable will be applied to ensure full compliance with the project requirements.

LIST OF ACRONYMS

Acronyms	Definition
DPWM	Discontinuous pulse-width modulation
FOC	Field oriented control
GaN	Gallium nitride
IMD	Integrated Motor Drive
KPI	Key Performance Indicators
PCB	Printed circuit board
PL	Programmable Logic
PS	Processing System
PWM	Pulse-width modulation
RHODAS	Reinventing High-performance pOwer converters for heavy-Duty electric transport
SiC	Silicon carbide
SoC	System on a Chip
SVM	Space vector modulation
SVPWM	Space vector pulse-width modulation
TIM	Thermal interface material
WBG	Wide-bandgap

1 INTRODUCTION

1.1 DESCRIPTION OF THE DOCUMENT AND PURSUE

This report describes the work carried out within the RHODaS project on the design and validation of the high-power hybrid T-type multilevel inverter. The document explains the overall structure of the converter, including sensors, modular power stages, mechanical design, housing, and integration aspects. It also provides a detailed account of the initial T-type design and the challenges encountered with the first GaN transistors, highlighting the lessons learned and their implications for the final prototype.

Furthermore, the report includes information on the initial inverter tests performed to verify switching behaviour and operation under different load points. Finally, it defines the comprehensive high-power inverter test procedures that will be conducted at BOSMAL to ensure full compliance with the project requirements.

1.2 WPS AND TASKS RELATED WITH THE DELIVERABLE

This deliverable refers to Task 5.2 and Task 5.3 included in WP5: Integration, testing and technical and environmental validation.

2 DESCRIPTION OF THE FINAL HYBRID HIGH-POWER T-TYPE MULTILEVEL CONVERTER

This chapter presents the design of the hybrid high-power converter (150 kW continuous) developed within the framework of project RHODaS. It provides a comprehensive description of the electronic components and their configuration, and the modular architecture of the converter. In addition, the chapter examines the mechanical structure, housing, and the integration of the system with the rest of the IMD.

It should be noted that, throughout this project, two versions of the high-power T-Type converter were constructed. The first design failed and led to the destruction of the converter. However, the experience gained enabled the development of a second design that delivered satisfactory results.

The design presented in this section corresponds to the final version of the converter. Nevertheless, this design is based on the initial version, the specific characteristics of which are described in Section 0.

2.1 STRUCTURE OF ELECTRONIC COMPONENTS

This section explains all electronic components e.g., PCBs and sensors to create a modular design. The high-power inverter itself includes the following elements:

- Three Modular Power Stages
  - Main Board with GaNs
    - GaN power semiconductors with separate drivers
    - GaN drivers with galvanic isolation
    - Optical interface, LV power supply, and temperature sensors
    - DC link capacitors
  - SiC power modules
    - DC-link auxiliary board
    - SiC driver board
- Current sensors
- DC link voltage sensor board
- SoC based control board (including resolver interface)

Figure 1 shows the overall structure of the final RHODaS high-power inverter.

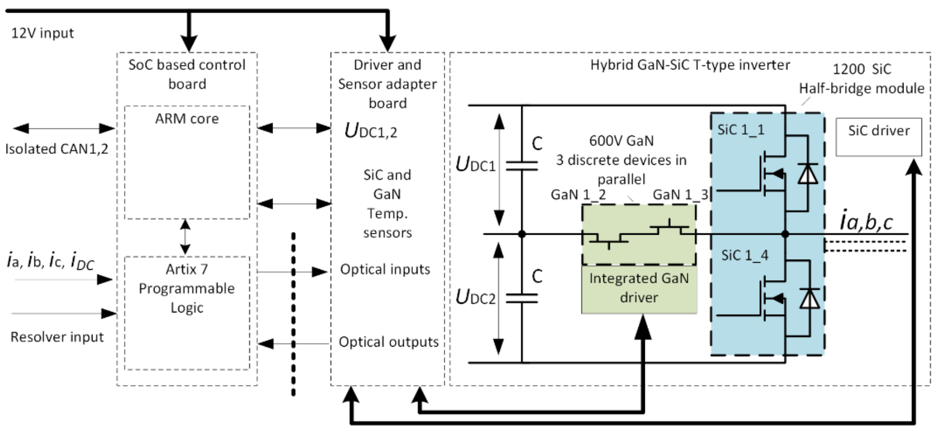


Figure 1 Overall structure of the final high-power inverter.

2.2 SENSORS

The developed SoC based control board offers the following sensor inputs:

- 4 x Current sensor front-end for: Closed loop Hall effect sensors like the LF 306-S or LF 505-S.
- Two DC-link voltage measurement (VDC1 and VDC2) inputs.
- 8 x 10k NTC temperature sensor inputs.
- 6 optical inputs based on digital optical receiver 660nm (905EM660KM001/002).
- 16 optical outputs based on Ratioplast Optical emitter 10Mbit/s 660nm (905SE660KM003) for 1mm plastic optical fiber.
- Two isolated CAN interfaces.
- One resolver interface based on the resolver-to-digital converter AD2S1200 (excitation frequency and voltage: 10 kHz, ~7 VRMS).
- JTAG, Open-drain and UART interface.

2.2.1 RESOLVER CALIBRATION

To calibrate the resolver, interface the excitation signal was adapted to stay within the limits of the selected resolver-to-digital converter AD2S1200 chip. The following table shows the minimum and maximum allowed output voltage of the Sin and Cos signals.

Signal name	Voltage range	Comment
Sin/Cos	2.92 – 4.09	(Typ. according to datasheet) [Vpp]
Excitation output	4.5V	Measured [Vrms]

Table 1 Resolver calibration values

The excitation output signal was reduced from 7 Vrms to 4.5 Vrms to avoid a degradation of signal (DOS) error resulting from exceeding the maximum allowed input voltage of the Sin and Cos inputs.

After calibration the absolute angular position can be read out via a SPI interface. The absolute position is set once and then the emulated encoder interface is used. This is necessary to avoid propagation delays due to the SPI communication. The inverter also checks if the motor is spinning during the startup phase. If the inverter detects a spinning rotor during the resolver initialization phase an error flag is set.

2.3 MODULAR POWERSTAGES

The whole inverter consists of three identical power stages, which are connected through copper wires for DC link connections at the bottom and flat cables for sensor and digital signals. The structure and functionality have already been described in detail. At this point, an overview of the final version and a description of the adjustments concerning the first and the second GaN stage should be provided.

Figure 2 shows an overview of one power stage and its components. The mechanical structure of the GaN section is described in section 3.1.1.

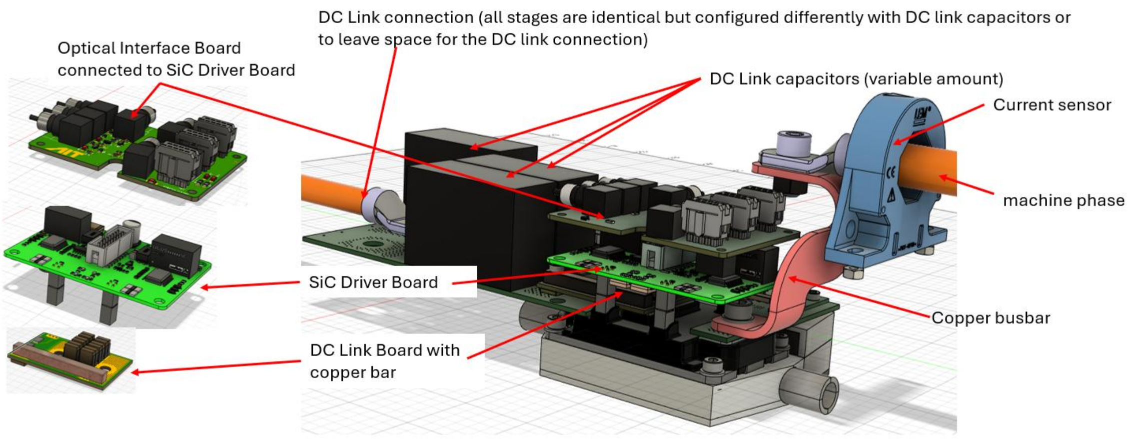


Figure 2 Overview of the modular power stage

The interface and SiC driver board are stacked together like a sandwich. The DC link board is guided with a copper busbar so that the connections can be directly routed through the current sensor. The shielding of the cable to the machine is only connected to the housing after the current sensor.

2.3.1 MECHANICAL STRUCTURE

The second design of the inverter with a new GaN stage (see Figure 3) had to rely on given mechanical parameters of the first design (see Section 0). The heat sinks with its drills were not changed, the housing was not changed, the SiCs and all other PCBs were not changed. Therefore, only minor changes were made to adapt the second GaN power stage to the
first design. A relevant difference is that the second design features bottom cooled GaNs.

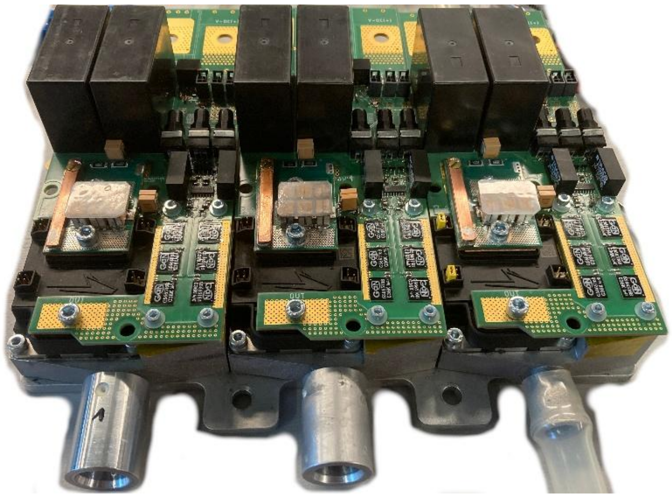


Figure 3 Second design of the inverter with a new GaN power stage

The GaNs are soldered on top of the board as shown in Figure 3. Below the GaNs a copper plate is directly soldered onto the PCB. On the one hand, this elevates the board, so that it exactly fits on the original heat sink design. On the other hand, it also distributes the heat from the bottom cooled GaNs equally on the plate, reducing the risk of overheating one GaN. The transistors are arranged in a common source topology, so all

GaNs share a common source potential. Therefore, no electrical insulation is required between the semiconductors themselves. The electrically insulated TIM is necessary but is only located between this copper plate and the water-cooled heat sink.

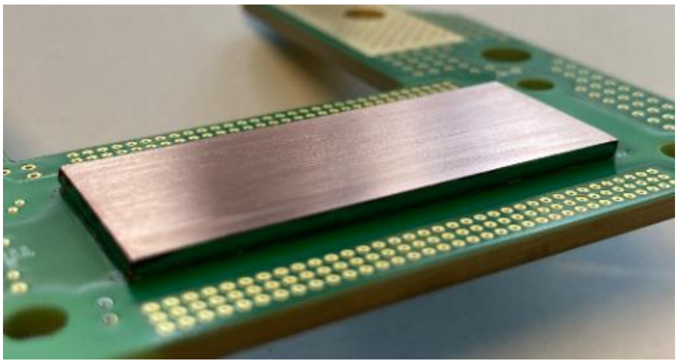


Figure 4 Copper plate soldered on PCB for thermal heat distribution

2.3.2 IMPROVEMENTS IN THE FINAL INVERTER DESIGN

The final version of the power converter incorporates several improvements derived from the lessons learned during the first prototype. The main modifications are:

- Replacement of pre-production GaN semiconductors with GS66516B-MR, bottom-side cooled.
- Shortened driver input traces and improved gate trace routing.
- Adapted layer arrangement.
- Inclusion of a DC-link mid-point connection.
- Permanent negative gate voltage supply.
- Provision for an additional gate capacitor to adjust switching speed.
- Optimized positioning of Ceralink and film capacitors for balanced DC-link capacitance.
- Updated connectors for simplified integration.

The permanent negative gate supply enables extended turn-off periods and simplifies the switching start-up procedure. An additional gate capacitor allows tuning of the switching dynamics when required. The final design employs a non-integrated isolated dual-channel driver (SI8275BBD-IS1, Skyworks Solutions) with a peak output current of 4 A. Optical inputs are positioned closer to the GaN driver, reducing the overall length of the driver input traces.

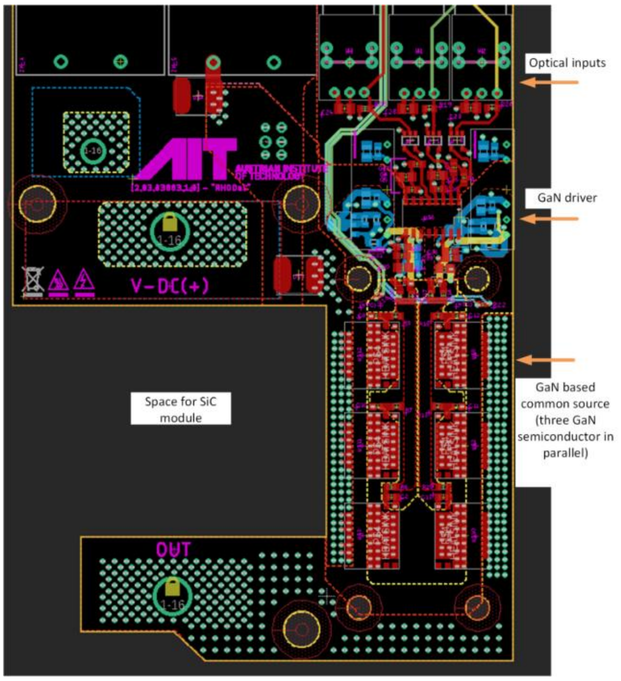


Figure 5 Part of the main power board PCB.

Figure 5 illustrates part of the main power board PCB. The optimized capacitor arrangement ensures equal distribution of capacitance between both DC-links. For the demonstrator, a DC-link mid-point input was also added to stabilize the input voltage during testing by enabling supply from two separate sources.

2.4 HOUSING DESIGN

The housing, where all components and the cooling system can be integrated, was designed in CAD. One challenge was to ensure that the assembly was feasible at all, with cooling being particularly difficult. In Figure 6, the housing with connections and all components is shown.

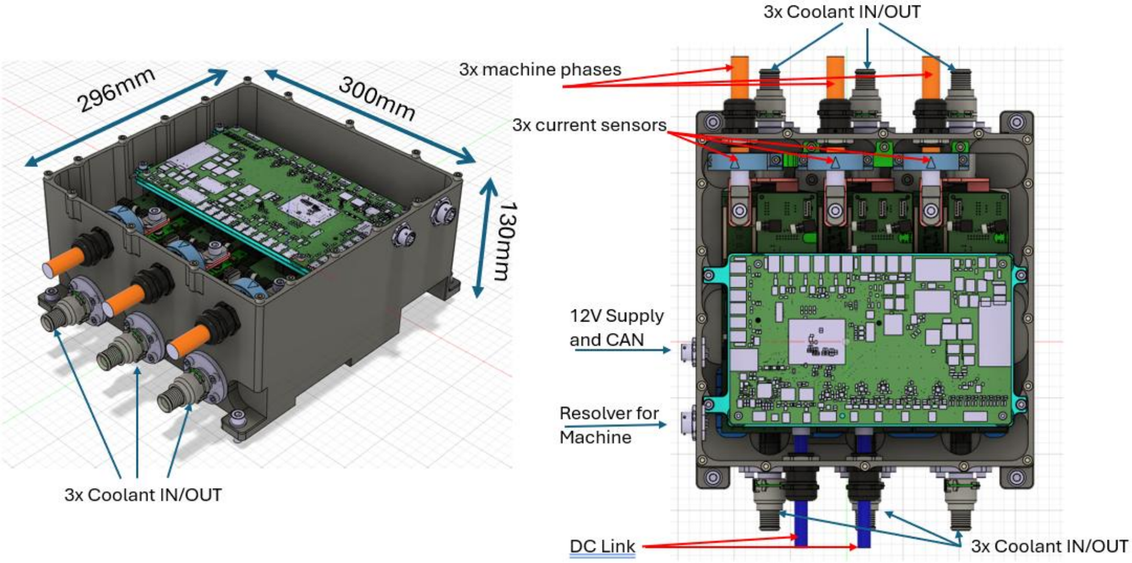


Figure 6 Overview of the Inverter with Housing

Figure 7 shows the cooling system in detail as it was implemented in the housing. Adapter pieces had to be manufactured and bonded to the 3D-printed coolers at AIT using 2K epoxy resin. The outside cooling connectors are designed to fit to automotive PC3 pluggable connectors.

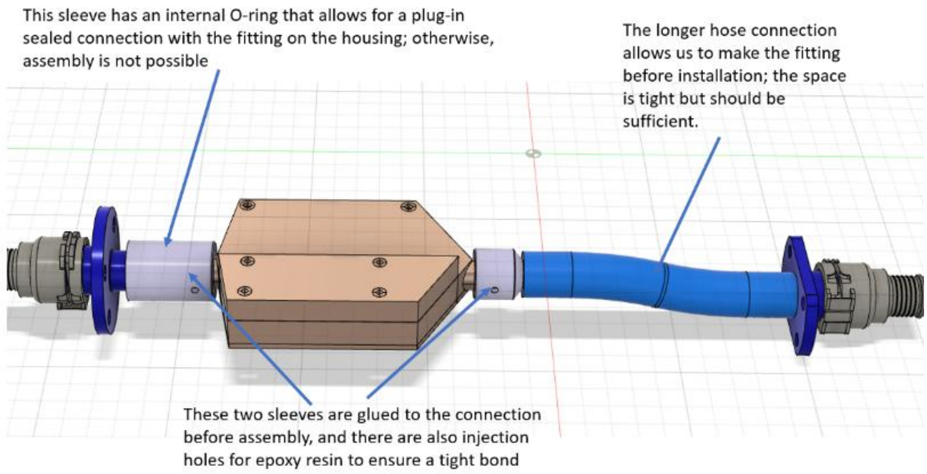


Figure 7 Cooling system in detail

Figure 8 shows the interior of the inverter when it is fully assembled. An additional base plate was necessary to mount all three heatsinks or fully assembled power stages together and provide stability. Copper connection bars transfer the current from the power PCBs to the terminals. The terminals can be directly screwed onto these bars through PG cable glands.

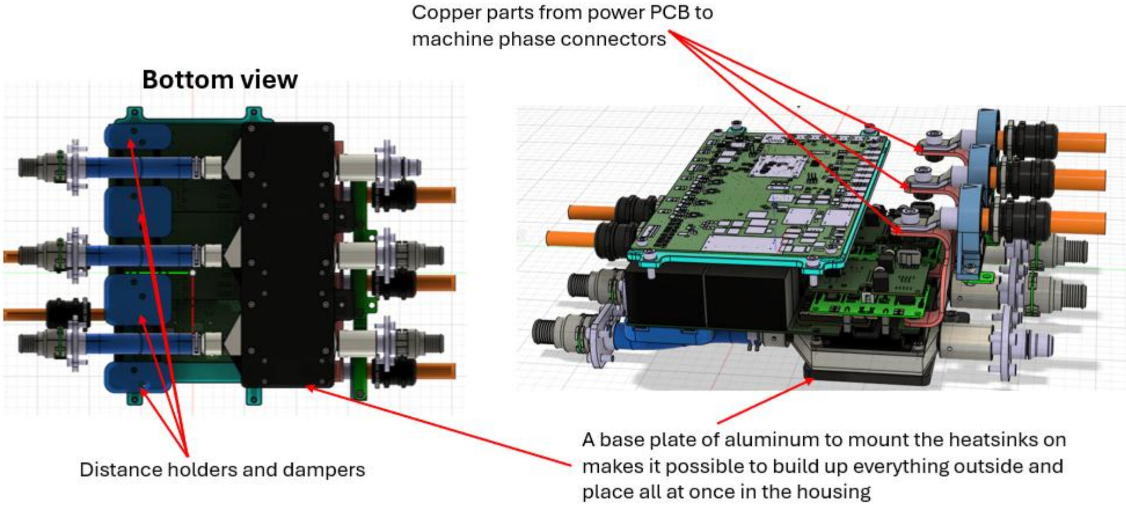


Figure 8 Housing interior of the Inverter

2.5 INTEGRATION OF THE INVERTER

In this section, a short report about the integration process is given. There were many details that had to be solved, which were very time-consuming. For example, the sealing of the connection adapters with epoxy resin for the cooling connectors or the positioning of the individual phases on the mounting plate. However, only the most important steps, insights, and results will be summarized here.

The integration steps were:

- Preparation of the heatsinks with threads for mounting on the base plate shown in Figure 9. Drilling M3 holes and cutting threads in aluminum was problematic because the available diameter was too small to create a stable thread. A conventional tap could not be used; instead, the threads were formed using specially modified screws to generate a M3 thread. The full thread was then utilized to prevent tearing out, eliminating the need for additional fixation in the base plate. Also, the mounting holes for the SiC modules could not be used as intended as previously mentioned, the aluminum was too soft. Therefore, special screws had to be manufactured.
- Bonding the connector adapters to the heatsinks. This was very tricky because everything had to be precisely aligned to fit through the O-ring connection. Also, the position of the modules had to be already fixed at this stage, which meant that the position of the M3 holes for the GaNs also had to be perfectly aligned. With pressure testing and mounting the heatsinks onto the cooling plate, this step took approximately two days to complete.

Figure 9 Coolers on baseplate with prepared TIM (left) and with mounted SiC modules (right).

- Isolating all critical areas with epoxy resin, such as the temperature sensors near the GaNs, and coating with protective lacquer. To ensure better access in the event of a failure, the second inverter was not coated with epoxy resin. All relevant areas had sufficient insulation clearance, but special care must be taken during repairs or other changes to the hardware to ensure that the mechanical conditions and insulation clearances are not inadvertently exceeded.

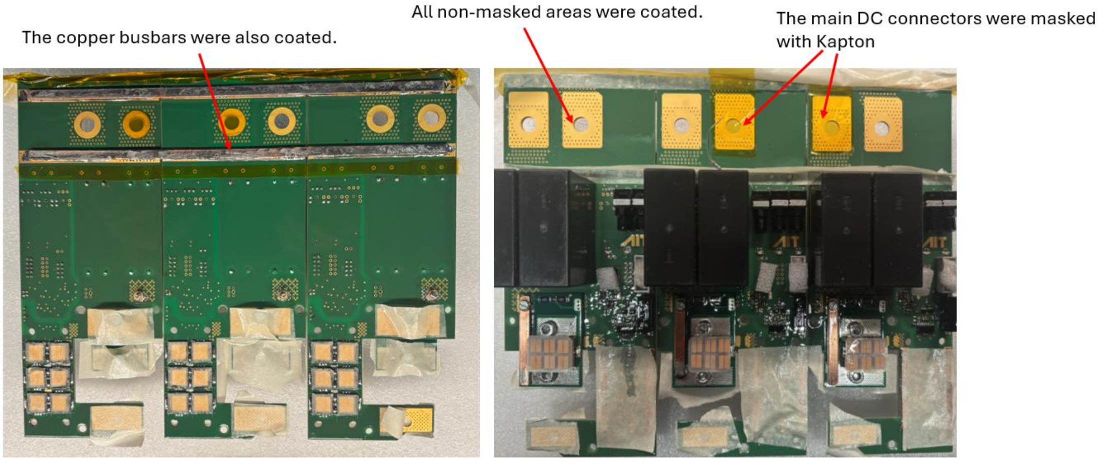
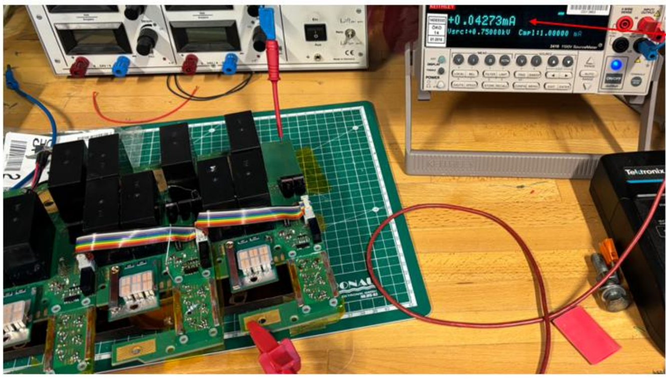


Figure 10 Isolation with coating

- Mounting all PCBs and testing in the assembled state. Insulation test, functionality test. Then disassembling for the last step. Also, the blocking voltage of the GaNs was tested with 750V, and the leakage current was measured to ensure that no damaged device was used. This can be seen in Figure 11 and had to be repeated after all steps that could have an influence, such as retightening the screws, pulse tests, or initial commissioning tests.



750V and a current of 42uA.

This measurement was made from DC/2 to phase output and always in two directions to ensure all GaNs are covered. The leakage current @750V was between 26uA and 56uA.

Figure 11 Blocking voltage test on assembled GaN Stages

- In the final GaN stage design, electrical insulation using Kapton tape was avoided due to its poor thermal conductivity. Instead, two layers of thermal interface material (TIM, TG-A1780, thermal conductivity 17.8 W/mK) were mounted on top of each other, resulting in a total thickness of 1 mm. This configuration provided a significantly lower thermal resistance for the GaN devices compared to the previous approach, while also allowing sufficient space for mounting the stage onto the heat sink. The selected TIM offers adequate electrical insulation, with a dielectric breakdown voltage of ≥ 8 kV/mm. However, its fragile consistency requires careful handling: once assembled, the GaN stage and heat sink should not be disassembled and reassembled with the same TIM, as hairline cracks may form in the material and compromise insulation reliability. This optimized thermal setup ensures both mechanical precision and reliable heat dissipation, supporting stable operation of the final inverter design.

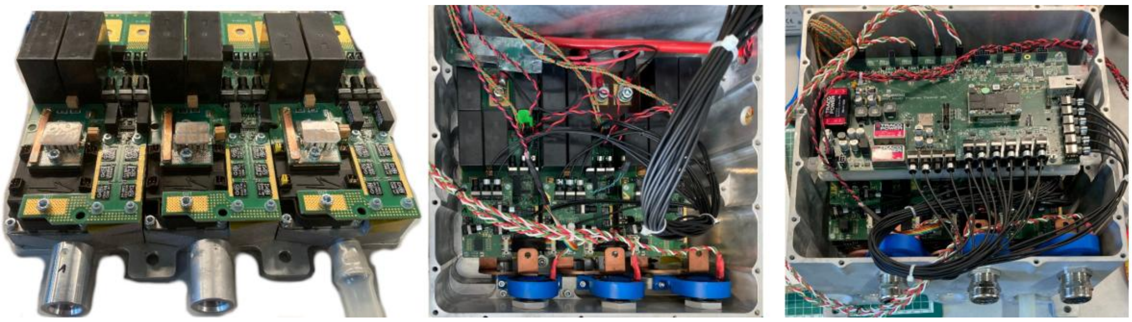


Figure 12: Inverter installed onto the heatsink (left), inverter inside the housing (center), inverter with control board (right)

Figure 12 shows the final inverter (without SiC drivers) installed onto the heat sink (left), mounted in the housing (centre), and together with the control board (right). The inverter can be installed into the housing without prior disassembly, which is very practical. The differences between the first and second inverter concern the GaN stage, and some changes to the position of the film capacitors. Those are arranged differently, so that in addition to DC+ and DC-, there is also a centre tap connection.

2.6 POWER DENSITY

To achieve a high-power density, assumptions had to be made that allow the inverter to be built in a more compact form.

The assumptions are as follows:

- A single PCB is placed on the SiC, integrating both the driver and the power supply. We have built the system in separate stacked layers to remain modular and save time, as developing an integrated PCB would be significantly more complex.
- In the final version, a customer-specific DC link capacitor can be used, specifically adapted for our inverter. This is a standard solution in the automotive industry but involves very high initial costs. In our inverter, this is represented as a single block of only one row of capacitors. This is realistic since specified capacitors can far exceed discrete capacitors in terms of pulse load and thermal performance.
- The connectors were shortened because the inverter is intended to be integrated into a different housing. As a result, we have omitted all unnecessary connection interfaces.

Figure 13 shows the result of the assumptions, with the volume transparently overlaid on the inverter.

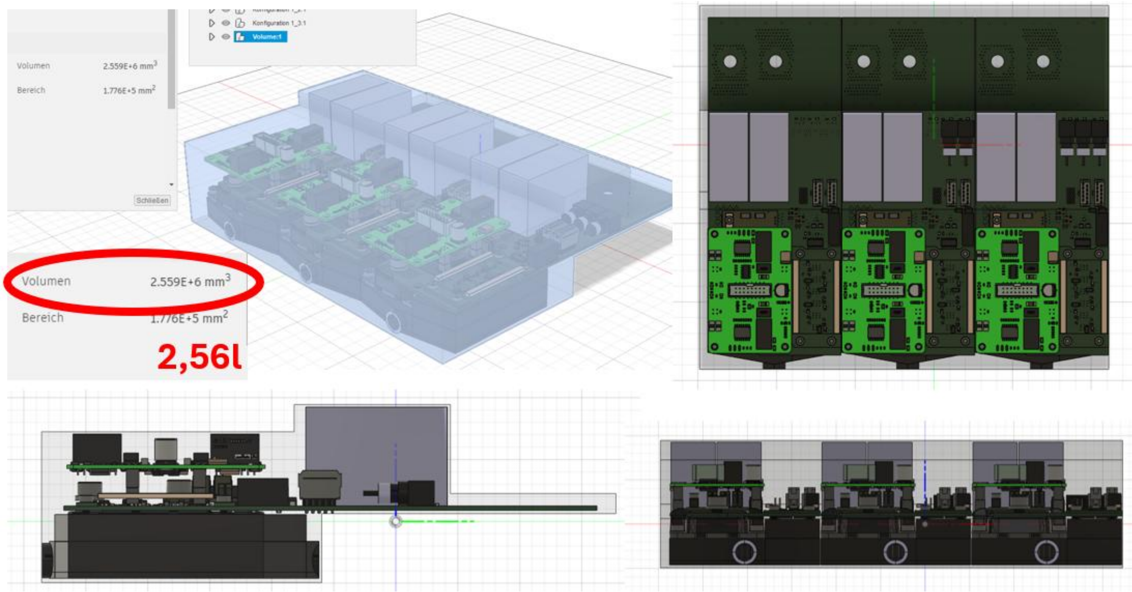


Figure 13 Illustration Power Density Calculation

The result of the volume calculation is 2,56 liters, which, with a possible power of 150kW, results in a power density of 58,6 kW/l.

3 INITIAL T-TYPE DESIGN

This section describes the first version of the inverter. The critical failures encountered in this initial design are outlined, together with the lessons learned and the objectives defined for the subsequent redesign. It is important to emphasise that the first and the final converter designs are highly similar; only the main power board differs slightly. In the initial design, GaN power semiconductors with integrated drivers were employed.

3.1 DESIGN DIFFERENCES

The main design difference between the initial and final versions of the converter was the replacement of the GaN transistors. The first prototype utilised pre-production GaN semiconductor devices, which exhibited several issues described in Section 3.2. These were subsequently replaced by GS66516B-MR transistors. As the initial devices incorporated integrated drivers, modifications to the gate-driver circuitry were required. In addition, the mechanical configuration of the GaN stage and its integration with the thermal management system differed slightly from the final design. These aspects are detailed below.

3.1.1 INITIAL MECHANICAL STRUCTURE

The first GaN stage was developed with mechanical components designed to ensure reliable thermal contact while maintaining galvanic isolation. The structure is shown in Figure 14. An additional spacer frame was manufactured to guarantee a constant distance between the GaN devices and the heatsink. The applied pressure was intended to prevent bending of the PCB and to ensure uniform mechanical contact.

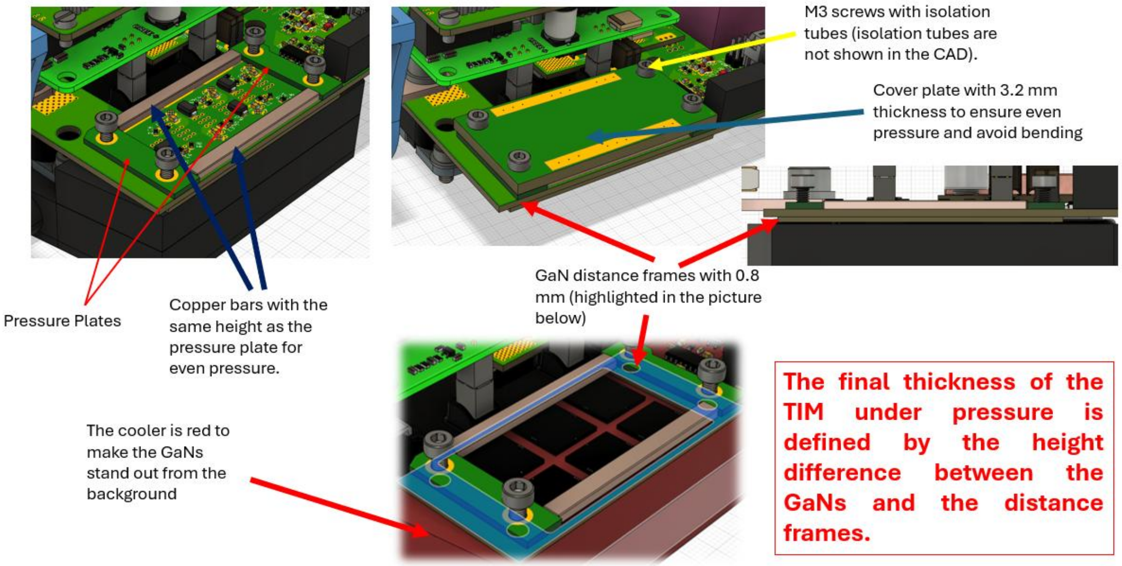


Figure 14 Initial Mechanical Structure of the GaN stage

3.1.2 INITIAL THERMAL DESIGN

In the initial thermal design, the TIM was applied and the GaN assembly pressed using pressure plates and spacer frames. An additional insulation layer of Kapton tape was introduced, as a single TIM layer was considered insufficient for electrical insulation. However, the thermal conductivity of Kapton is poor, and this limitation was accepted in the first design. The thermal arrangement of the inverter was particularly complex, since the assembly had to fit within a tolerance of ±0.05 mm. Deviations beyond this tolerance could result in inadequate thermal contact or induce bending stress on the PCB carrying the GaN devices.

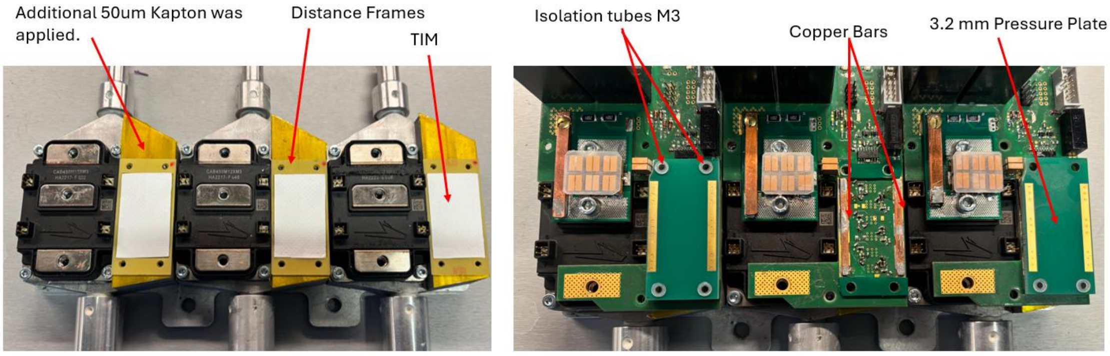


Figure 15 Applied TIM with distance frame (left) and assembled GaN stages (right) for the first GaN stage. The second inverter does not have Kapton tape and doesn't need the distance frames. Therefore, the second design was simplified compared to the first one.

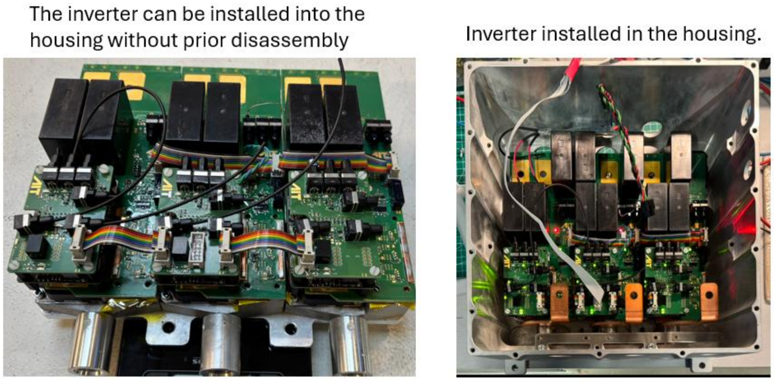


Figure 16 Assembled first inverter without control PCB

3.2 ISSUES WITH INISITAL GAN TRANSISTORS

3.2.1 LACK OF NEGATIVE VOLTAGE

Due to the driver concept, it is not possible to maintain negative gate voltage during long turn off periods (time constant about 470µs). There are two concerns which had to be clarified.

- As expected, no significant issues arise in this regard. The behaviour is described in detail in deliverable 5.3.
- First switch with no negative voltage. Figure 17 shows a fist turn on and off with no negative voltage at all. With a current of about 60A there is a desaturation state of about 400ns.

CH1 (yellow) : Gate Voltage GaN CH3 (Blue) : Current over GaN Stage

CH2 (Green) : Voltage over GaN Stage CH4 (Pink) : Control Signal GaN

Figure 17 Turn-On and Turn-Off Under Load Without Negative Gate Voltage

In practice, no significant issues arise if there is no malfunction in the machine or the inverter. However, it is essential to always prevent a high current from being switched off through the GaNs without prior switching. If the GaNs are always switched complementarily in 2-level operation, a negative voltage will always be present at the driver in case of an unforeseen condition. In 3-level operation with a machine, the large inductance of the machine ensures a safe operation at start-up of current. However, if a machine fault or an overcurrent occurs in this stage, it is more likely to destroy the GaNs, even though it is generally almost impossible to survive a full short circuit as it is possible with the SiCs.

3.2.2 UNFORSEEN SHORT CIRCUIT AND VOLTAGE WITHSTAND CAPABILITY

During the initial tests, it was observed that some GaNs exhibited significantly higher leakage currents at 750V compared to others. The measured range varied between approximately 6 µA up to 25 µA at 750V. However, as shown in Figure 11, all devices passed the initial voltage test before assembly.

During the first functional test, a fault occurred in which a desaturation event was also triggered on the SiC Module. The fault analysis revealed that one GaN had apparently been destroyed, showing a short circuit between the gate and source. At first glance, the three complementary GaNs appeared to be functional, as they were still able to switch, but were replaced as a precaution.

After reassembly, higher leakage currents were observed in other bridges as well, occurring in the range of 150V to 250V, exceeding the 1mA current limit of the test equipment. To identify the faulty GaNs, a constant voltage was applied using a more powerful power supply. After approximately one minute at 200V, two GaNs began to generate heat. These were removed, and the test was repeated. Subsequently, another GaN experienced a sudden short circuit at around 300V and exploded. This caused no damage because the heat sink was not mounted, see Figure 18.

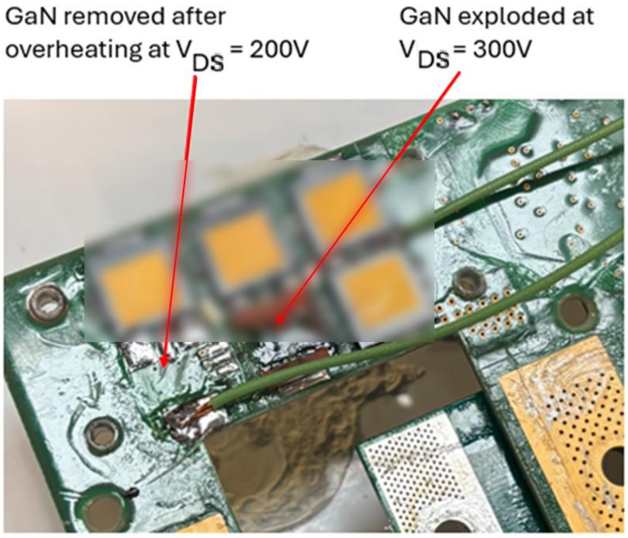


Figure 18 Turn-On and Turn-Off Under Load Without Negative Gate Voltage

This test method was necessary because non-destructive replacement of the GaNs was not possible, and independent testing of each device in parallel operation could not be done. After replacing all faulty GaNs, the inverter appeared to function normally and was further tested successfully at 800V DC-Link with low current.

3.2.3 FAULTY SAMPLES ANS MISSING GROUND CONNECTION

After the initial tests with low current, the inverter was prepared for installation into the housing. Since we had learned that our GaN samples were not entirely unproblematic and would therefore no longer be produced, everything was rechecked.

Among the 12 already installed GaNs, no changes in internal resistance or voltage withstand capability were observed after the initial tests. However, it was noticed that not all GaNs had proper connections between the source terminals. Out of the 18 GaNs, three showed either no connection or a connection with excessively high resistance between the source terminals and the cooling pad.

To ensure that no pre-existing damage was overlooked, the switching behaviour of all affected GaNs was tested separately. The results showed that all these GaNs could switch and exhibited no increased internal resistance. The measurements were conducted by switching only one gate at a time from the three parallel GaNs. This was achieved by desoldering the respective gate resistors and shorting the gate.

However, it remained uncertain how high the leakage current was at 750V, as this could only be measured for all GaNs in parallel. Additionally, it could not be ruled out that the missing ground connections indicated either pre-existing damage or a manufacturing defect.

At this point, only eight GaN samples remained. Measurements on these GaNs revealed that only four had no missing ground connections. However, only one spare GaN was found where there was no ground connection to the housing, but two others showed missing connection to one of the solder ground pads. In the soldered state of the GaNs, the ground pads are also connected through the PCB, making it impossible to determine whether there is a missing connection between them. At least the switching tests and the gate switching behaviour showed no significant abnormalities. It is possible that under switching conditions in inverter operation, this could lead to failure or unintended turn-on.

3.3 DESTRUCTION OF THE INITIAL INVERTER

During the first loads points, the inverter failed and created a short circuit. The fault occurred during the last operating point in table 5 which was 400V and 90A output current. The exact cause remains unclear, as no unusual power increases or temperature rises were recorded before the failure. Therefore, a sudden short circuit must be assumed.

In any case, after the inverter was exposed to thermal cycling on the test bench, which could have caused pre-existing damage to develop into a failure. This operating point had already been tested before, with only the machine speed being adjusted, which has no significant impact on the load of the GaNs.

Figure 19 shows the PCB with the destroyed GaNs and an opened SiC module, which was also destroyed.

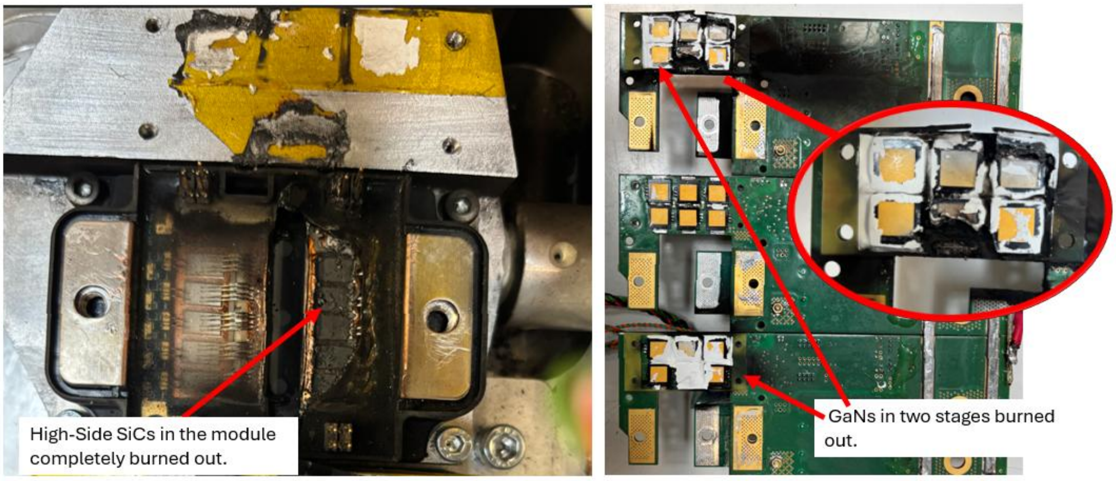


Figure 19 Turn-On and Turn-Off Under Load Without Negative Gate Voltage

The desaturation of the SiC module was tested beforehand, but in this failure case, it was unable to protect the high-side SiCs. The cooler has minor damage and marks and is replaced with a spare part for the second inverter.

3.4 CONCLUSIONS REGARDING INITIAL GAN SEMICONDUCTORS

During the integration phase of the first inverter prototype, it was communicated that the used pre-production GaN semiconductors were discontinued. Several devices failed either prior to installation or after the first load cycles. Although a functional inverter comprising 18 GaNs was eventually assembled and tested following extensive troubleshooting and replacements, catastrophic failure occurred after only a few test points. This resulted in the destruction of 12 GaNs, with the remaining 6 considered at high risk of latent damage, as well as the destruction of the GaN PCB and one SiC module.

3.4.1 KEY LESSONS LEARNED

- **High risk in bridge short-circuit topologies**. Implementing an inverter topology where bridge short circuits can occur is inherently a high-risk when using GaNs. To our knowledge, no reliable desaturation protection for GaNs has been successfully developed and tested for similar applications. Therefore, it is crucial to avoid a short circuit under any circumstances. Additionally, overcurrent should be avoided, as they can cause overvoltage when switched off. This is particularly important in our application, as overcurrent in the GaN branch during turn-off can generate excessive overvoltage due to the higher inductance of the GaN path, which may potentially destroy the GaNs even if the current itself is not yet too high. Unfortunately, this cannot be entirely ruled out in practice, especially during commissioning.

- **Absence of negative gate drive voltage.** The lack of a negative gate drive voltage increases the risk of unintended turn-on in inverter operation. Given the already high risk associated with GaN failures, a stable negative gate voltage should be provided to maximize reliability.
- **Insufficient voltage withstand capability due to pre-damage.** Even though every GaN was tested for voltage withstand capability and leakage current before installation, premature failures still occurred in operation. While additional testing with current and pre-exposure to thermal cycling before installation could theoretically improve reliability, the effort required would be extremely high, and the probability of identifying all pre-damaged devices would still not be sufficient.
- **Missing ground connection.** This issue is also likely to have an influence on reliability and could have been also detected through pre-testing including thermal cycling. However, as with the previous point, the required testing effort would be very high, and the effectiveness of such screening could also not be ensured.

3.4.2 IMPLICATIONS FOR THE FINAL DESIGN

These findings underscore the importance of utilising the most reliable GaN devices and gate drivers available. The second inverter, incorporating a redesigned GaN stage, was developed specifically to address these shortcomings. By integrating a permanent negative gate supply, improved driver circuitry, and optimised mechanical and thermal arrangements, the final design successfully avoided the critical issues encountered in the initial prototype. The inverter operated as expected and demonstrated stable performance. Although the redesign introduced significant delays to the project timeline, it ultimately ensured a robust and functional converter architecture.

4 INITIAL POWER CONVERTER TESTS

This section includes a description of the inverter tests which are performed in the drive lab of AIT. These tests should ensure that the inverter is able to perform the basic operations and can provide the defined output current. First, the basic 2-level switching operation was tested, which only includes the SiC part of the inverter. Then, the 3-level operation was tested were both SiC and GaN semiconductors are in operation. Figure 20 shows the first test setup. This test setup includes an asynchronous motor which acts as a first load to check the basic control and the connection between the control board and inverter. After those initial measurements were successful the first inverter was tested on the testbench.

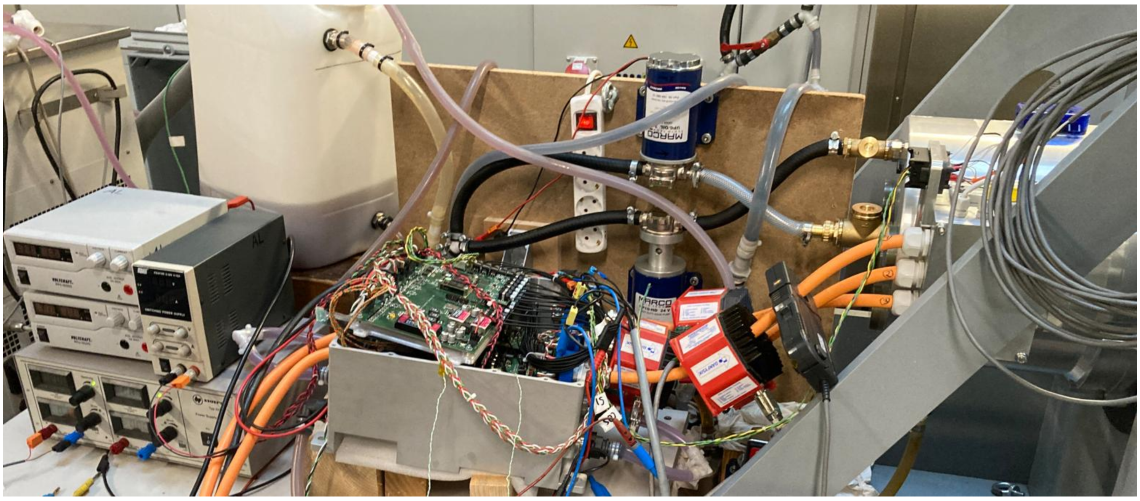


Figure 20:Test bench setup of the final inverter

Table 2 lists the optical connections between the control board and the inverter.

Inputs	**Description**
SiC fault input [1-3]	Active low, indicating a desaturation fault.
SiC digital temperature [1-3]	PWM temperature output 0°C – 175°C (4.6kHz – 30kHz)
Outputs	
PWMXH/PWMXL [1-12]	Inverted and non-inverted gate signals.
SiC PWM enable	Enables the SiC driver.
GaN PWM enable	Enables the GaN driver.
SiC fault reset	Resets the SiC driver

Table 2 Optical connections between the inverter and the control board.

Figure 21the labelled optical connectors and the PWM wiring representative for all inverter legs.

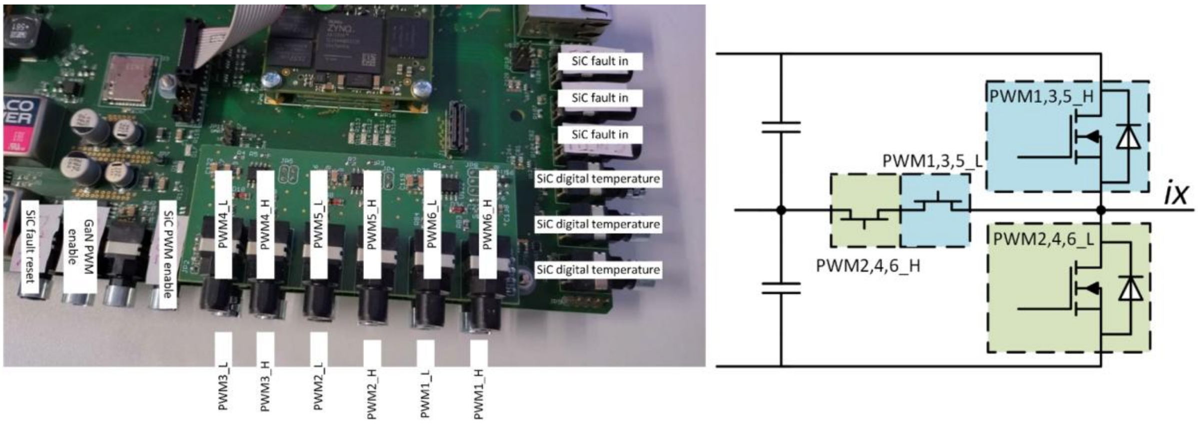


Figure 21:Optical inputs and outputs of the control board (left); PWM output wiring of on phase of the T-type inverter (right)

4.1 SWITCHING OPERATION

The control system of the second inverter was not modified, so after testing each GaN phase separately for functionality using double pulse tests and switching tests under load, the second inverter was tested on the test bench. The physical setup can be seen in Figure 19. The voltage and current curves look as expected. In Figure 22 an exemplary measurement of two phase to phase voltages and two-phase currents are shown. Figure 22 shows the phase-to-phase output voltage in 3-level operation at 60A peak phase current. Figure 23 and Figure 24 show the voltage levels during a transition between 2-level and 3-level operation. In the corresponding current it can be seen that the harmonics of the current curve immediately decrease, once the 3-level mode is active.

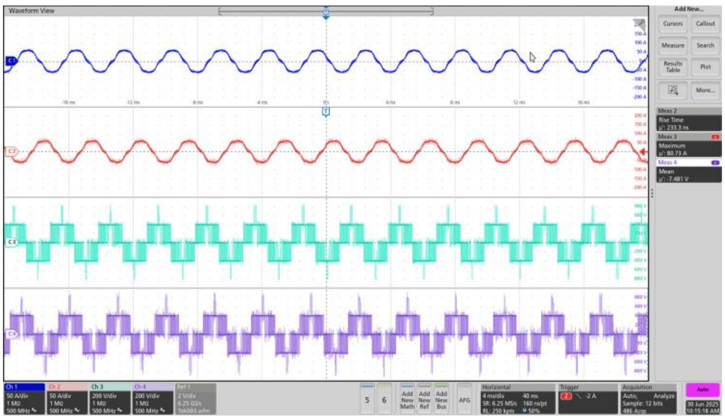


Figure 22: Phase currents (blue and red); phase to phase voltages (turquoise and purple)

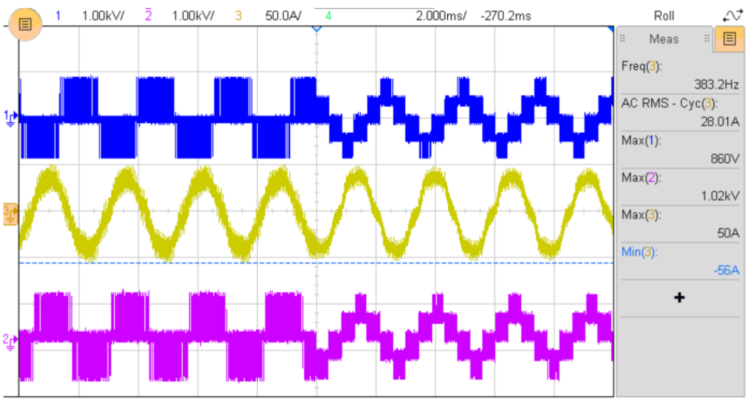


Figure 23:Transition between 2 level and 3 level operation

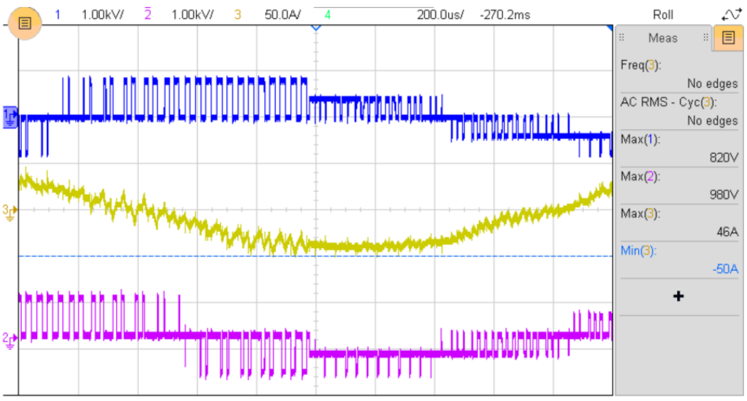


Figure 24: A detailed look at the voltage levels of the transition between 2 and 3 level operation mode

4.2 LOAD POINTS

This section shows different load points conducted with the PMSM provided by Valeo Siemens. Table 3 shows the parameters of the PMSM. For these tests the inverter was water cooled, and all heat sinks were connected in series to reduce the complexity of the water-cooling system. The DC-link voltage was set to 400V before tests at 800V and 1000V were conducted.

Table 3 PMSM parameters.

Parameter	Value
Max. Speed	10500 rpm
Rated power	183 kW
Motor maximal temperature: (Class H)	180°C
Power factor (Cos Phi) @ continuous performance	[191 Nm,8400 rpm]: 0.92 [166 Nm,10500 rpm]: 0.9962
Stator resistance Rs	0.0149 Ω
Inductance L	200 – 500µH

The inverter efficiency, torque and speed were measured using a torque measurement shaft type 4503B from Kistler. The input and output power of the inverter was measured with the help of a power analyser type WT3000 from Yokogawa. The data was recorded using a data acquisition system from IMC. The maximum speed of the load machine is limited to 8000rpm.

The final inverter was tested on the testbench with the electric motor by Valeo Siemens. Initially tests with 2-level and 3-level SVPWM modulation were conducted at 800V. Measurements at 1000V were done on one test phase to make sure, that the inverter will withstand 1000V DC link. After those measurements were successful, the complete inverter was also tested at 1000V and finally duration tests at 800V were done. There were no issues or problems with the new inverter. This was mainly because a lot was learned from the first version of the inverter and the tests that were performed had enough safety margin in terms of temperature and current capability.

Table 4 shows the measurement results of the final inverter on the testbench. The phase current was set to a desired peak value, and the speed of the load machine was set to a constant value. Depending on the DC link voltage the resulting torque, the input power and the inverter efficiency were measured.

Table 4: 3-level operation mode; 800V DC link at different phase currents and speeds

Peak Phase current Iq [A]	Speed [rpm]	Inverter efficiency [%]	Te [Nm]	Pin [W]	UDC [V]	Machine efficiency [%]	Temp Start of GaN [°C]	Temp End of GaN [°C]
10	250	80.6	7.6	335	800	73	26	27.5
20	250	86.2	16.17	592	800	83	26	31.5
30	250	86.5	24.4	857	800	86	27	38.5
40	250	86.6	32.8	1133	800	87.8	27	49
50	250	85.2	41	1427	800	87	27	65
60	250	84	49.4	1747	800	87	27	87
10	500	89.5	7.5	607	800	72	26.5	28
20	500	92	15.9	1077	800	83.5	26.5	32
30	500	92.4	24.2	1564	800	87.5	27	39
40	500	92.5	32.5	2060	800	89	27	49
50	500	92	40.8	2570	800	90	27	63
60	500	92.1	49	3100	800	90.5	27	85
10	1000	95	7.5	1104	800	75	27	27.5
20	1000	96	15.6	1983	800	85.7	25.5	31
30	1000	96.3	23.8	2890	800	89.5	26	38
40	1000	96.2	32	3800	800	91.5	26	47.5
50	1000	95.8	40.2	4750	800	92.4	26	61
60	1000	95.4	48.3	5700	800	93.1	26	83
10	2000	97	6.6	1923	800	73.9	26	27
20	2000	97.9	14.8	3688	800	86.2	26	31
30	2000	97.9	23.07	5460	800	90.2	26	37
40	2000	97.9	31.2	7233	800	92.3	26	46
50	2000	97.8	39.4	9025	800	93.5	26	58
60	2000	97.6	47.5	10815	800	94.2	26	76
10	3000	97.7	6.6	2817	800	75.6	26	27
20	3000	98.4	14.8	5440	800	87.2	26	31
30	3000	98.5	23	8056	800	91	26	37
40	3000	98.6	31.1	10657	800	93	26	44
50	3000	98.5	39.2	13290	800	94.2	26	55
60	3000	98.5	47.4	15914	800	94.9	26	68
10	3500	97.8	6.6	3227	800	76.9	26	27
20	3500	98.5	14.84	6264	800	88	26	31
30	3500	98.6	22.9	9300	800	91.6	26	36
40	3500	98.7	31	12330	800	93.5	26	44

50	3500	98.7	39.1	15360	800	94.6	26	53
60	3500	98.8	47.2	18370	800	95.3	26	66
30	4000	98.8	22.8	10512	800	92	26	36
50	4000	98.8	38.9	17412	800	94.8	26	52
60	4000	99	47	20830	800	95.5	26	63

Table 5: 2-level operation mode at 800V DC link

Peak Phase current Iq [A]	**Speed [rpm]**	**Inverter efficiency [%]**	**Te [Nm]**	**Pin [W]**	**UDC [V]**	**Machine efficiency [%]**
30	250	75.98	23.91	970.56	800	84.9
60	250	82.3	48.74	1784	800	87.3
90	250	83.2	73.2		800	86.1
120	250	83.8	97.15	3591	800	84.5
150	250	84.1	120	4560	800	82
180	250	83.69	142.29	5557.1	800	80.1
200	250	83.67	156.6	6249	800	78.4
220	250	83.17	170.47	6960	800	77.12
30	500	86.668	23.5083	1680	800	84.5
60	500	89.95	48.39	3145.81	800	89.55
90	500	90.3	72.9	4699.22	800	89.96
120	500	90.58	96.78	6251.83	800	89.48
150	500	90.577	119.81	7822	800	88.54
180	500	90.29	141.91	9425.95	800	87.31
200	500	90.11	156	10495	800	86.41
220	500	89.923	169.8	11570	800	85.4525
30	1000	92.82	22.87	3041.97	800	84.8284
60	1000	94.4354	48.49	5922.97	800	90.7922
90	1000	94.82	72.93	8738	800	92.1784
120	1000	94.9	96.7355	11556.38	800	92.36
150	1000	94.95	119.63	14345.41	800	91.97
180	1000	94.6	141.34	17081.45	800	91.6
200	1000	95.13	143.32	18732.62	800	84.22
220	1000	95.03	168.59	20511.75	800	90.57
30	2000	97.3	23.49	6004.41	800	84.2
60	2000	97.73	48.13	11388.74	800	90.57

90	2000	97.82	72.19	16713.72	800	92.47
120	2000	98.31	95.48	21835.94	800	92.15
150	2000	98.16	117.85	26958.08	800	93.28
180	2000	97.9	139.12	31903.73	800	93.29
200	2000	97.8	152.57	35095.2	800	93.0985
220	2000	97.71	165.57	38217.87	800	92.86
30	3000	98.23	23.2	8776.3	800	84.52
60	3000	98.5	47.36	16612.64	800	90.94
90	3000	98.97	71.18	24308.22	800	92.95
120	3000	98.87	94.05	31884.66	800	93.73
150	3000	98.74	115.82	39187.7	800	94.03
180	3000	98.54	136.76	46305.83	800	94.1621
200	3000	98.47	149.94	50839.88	800	94.01
220	3000	98.44	162.73	55276.66	777	93.96
30	3500	98.53	22.99	10053.1	800	85.05
60	3500	99.18	46.97	19018.81	800	91.27
90	3500	99.12	70.59	28006.54	800	93.21
120	3500	99.01	93.02	36626.79	800	94.0148
150	3500	98.89	114.74	45071.41	800	94.36
180	3500	98.76	135.52	53224	784	94.4951

The measurement results from the tables are also visualised in efficiency maps in Figure 25. A comparison of inverter efficiency between 2-level and 3-level operation mode is shown in Figure 26. It can be seen, that especially at lower speed and torque the 3-level operation mode is more efficient than the 2-level operation mode.

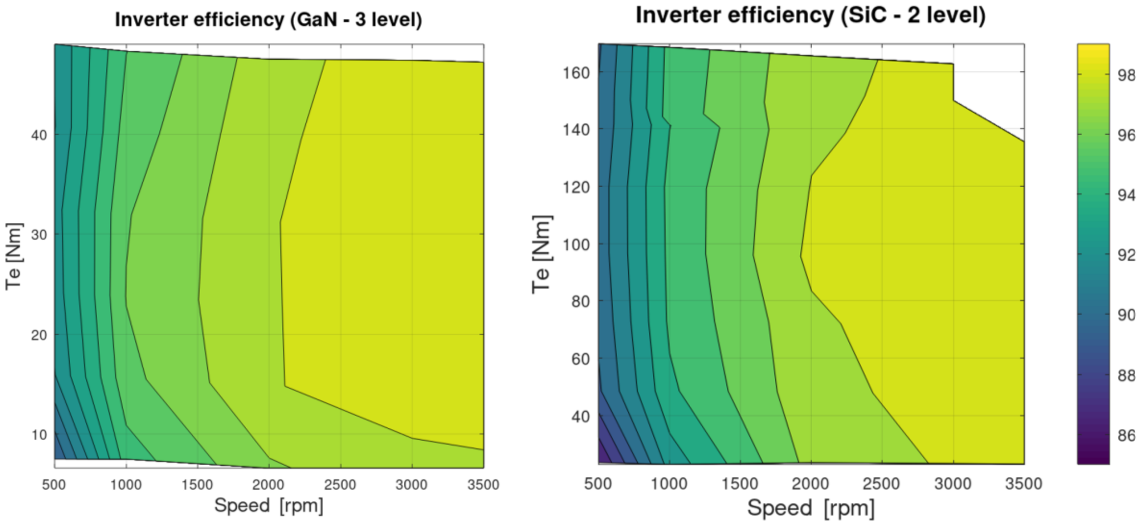


Figure 25: Efficiency map of 3-level and 2-level operation

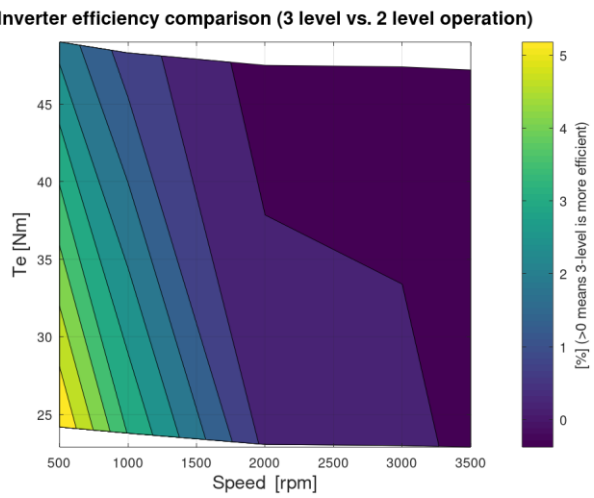


Figure 26: Comparison of inverter efficiency between 2-level and 3-level operation mode, showing that at lower speeds the 3-level operation the inverter is 2-4% more efficient compared to 2-level operation.

Table 6: 2-level and 3-level operation mode at 1000V DC link

Peak Phase current Iq [A]	Speed [rpm]	Inverter efficiency [%]	Torque [Nm]	Pin [W]	UDC [V]	Machine efficiency [%]	Losses Calculated [W]	Total efficiency [%]	Operation level mode
10	1000	92.14	7.94	1242.76	1000	72.6824	97.6809	66.97	3
20	1000	94.86	16.22	2144.8	1000	83.5	110.243	79.21	3
30	1000	95.45	24.5	3063	1000	87.7426	139.367	83.75	3
40	1000	95.4	32.735	3996.5	1000	89.904	183.839	85.77	3
50	1000	94.9863	40.97	4946.53	1000	91.31	248.004	86.73	3
60	1000	94.715	49.1987	5901.57	1000	92.1727	311.898	87.30	3
20	1000	86.47	7.22	1412.20	1000	61.96	191.043	53.58	2
60	1000	93.49	40.21	5122.14	1000	87.93	333.199	82.21	2

Table 6 shows the results of the endurance test. During these tests the maximum continuous current of 60A peak was applied in 3-level mode to not exceed the maximum temperature of the PCB and the semiconductor. In 2-level mode a maximum current of 220A peak was applied.

Figure 27 shows the results of the measured temperatures during the endurance test. It can be seen how the measured temperature of the GaN increases each time the current is increased. The time constant until the temperature on the GaN stabilizes is approximately half a minute. The NTC which was installed close to the GaN does not reflect the junction temperature of the GaN. They are mounted too far away because a minimum distance must be maintained to ensure sufficient insulation clearance. Therefore, an additional isolated type K thermocouple was mounted on top of the GaN semiconductor. Furthermore, a thermocouple was mounted on a DC link capacitor. The temperature of the DC link film capacitor rises slowly and has not yet reached its steady-state temperature. However, the duration tests showed that the inverter can handle the rated continuous currents.

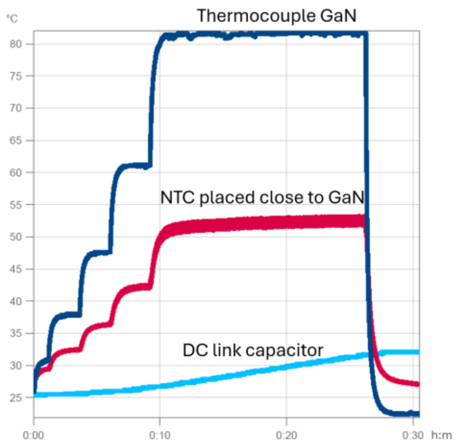


Figure 27: Measured temperatures at rising load currents up to 60A peak: thermocouple mounted directly on one GaN (dark blue), NTC placed close to the GaN (red), thermocouple on the DC link capacitor (light blue).

5 DEFINITION OF HIGH-POWER INVERTER TESTS

5.1 TEST BED LAYOUT AND INSTRUMENTATION

This section describes the prototype high-power inverter test program foreseen to be performed in the Mechanical Testing Laboratory at BOSMAL. For the purpose of providing realistic alternating current (AC) load, the high-power inverter will be integrated with an electric permanent magnet synchronous motor (PMSM) and coupled with a 2-speed, single output shaft gearbox. The entire powertrain unit constituting an e-axle will be installed on the test bed consisting of AC dynamometer commanded by AVL automation system capable of transient operation and simulation of the road loads. The e-axle unit will be powered by the AVL, E-STORAGE, the bi-directional direct current (DC) source/sink unit dedicated to high electrical power demand.

5.2 TEST METHOD

In order to determine the high-power inverter efficiency and losses the electrical parameters including voltage and current values will be acquired by the power analyser connected at the input and output of the inverter. The elaborated test program was based on a comprehensive review and analysis of existing standards related to the next generation power inverters developed for electric mobility under the RHODaS project. Since the novel solution of RHODaS power inverter remains at prototype stage, certain test procedures were modified and customized based on the engineering judgement and experience of the RHODaS Partners. The test protocol is described in the points below.

5.2.1 INVERTER TEST – MEASUREMENT OF LOSS, EFFICIENCY AND CONVERSION RATE

This test is based on the standard ISO 21782-3:2019(E). The scope of the test is to operate the inverter under the specified conditions and to measure the loss and efficiency of the inverter in order to ensure that the inverter performance is as designed.

Test procedure:

- The test inverter shall be operated at specified output-current points for the operating time defined in Table 7. Inverter input power and output power shall be recorded - each average of the last one second of the records shall be used.
- The efficiency, conversion rate and loss shall be calculated by using the following formulas:

$$\eta_{\mathrm{i}} = \frac{P_{\mathrm{io}}}{P_{\mathrm{ii}}} \times 100 \tag{5.1}$$

$$\eta_{\mathrm{i\_conv}} = \frac{P_{\mathrm{io\_fund}}}{P_{\mathrm{ii\_mean}}} \times 100 \tag{5.2}$$

$$P_{\mathrm{il}} = P_{\mathrm{ii}} - P_{\mathrm{io}} \tag{5.3}$$

where:

ηi	- the efficiency of the inverter including harmonics and ripples (in %)
Pio	- the inverter output power (in W)
Pii	- the inverter input power (in W)
ηi_conv	- the conversion rate of the inverter (in %)

Pio_fund	- the fundamental inverter output power (in W)
Pii_mean	- the average inverter input power (in W)
Pil	- the loss of the inverter (in W)

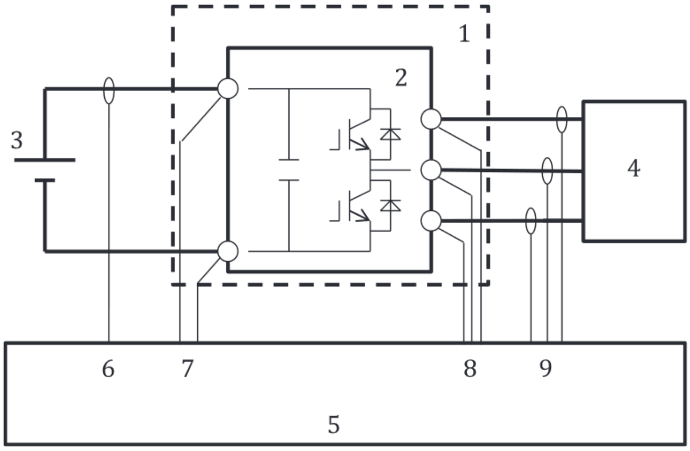


Figure 28 Diagram for measurement of loss, efficiency and conversion rate of the inverter

where:
1 device under test
2 inverter
3 DC power supply
4 AC load
5 spectrum analyser/power meter
6 inverter input current (in A)
7 inverter input voltage (in V)
8 inverter output voltage (in V)
9 inverter output current (in A)

Table 7 Conditions for measurement of loss, efficiency and conversion rate of the inverter

Test conditions	Values	Remark
Inverter input voltage	Maximum voltage for unlimited operating capability as defined in ISO 21782-1:2023, 3.14.	
Output current	The points as defined in ISO 21782-1:2023, Figure 1 — "a", "b"	
Ambient conditions	Unless otherwise specified, all tests shall be performed at RT of (23 ± 5) °C and with a relative humidity between 25 % to 75 %	
Coolant temperature	Maximum temperature for unlimited operating capability	— In case of liquid cooling — Ethylene glycol and propylene glycol as examples of coolant — If technically feasible, the tests shall be performed at coolant temperature of 65 °C. Otherwise the deviation shall be documented in the test report.
Coolant flow rate	Liquid: Minimum flow rate for unlimited operating capability Air: Minimum flow rate for unlimited operating capability	
Output frequency	Rated frequency (fr) as defined in ISO 21782-1:2023, 3.21.	

Switching frequency	In accordance with the designed frequency	
Operating time	— The operating point "a": 2 s or 10 s — The operating point "b": 1 800 s	

5.2.2 INVERTER TEST – TEMPERATURE RISE TEST

This test is based on the standard ISO 21782-3:2019(E). The scope of the test is to operate the inverter under the specified conditions and to measure the temperature rise in the inverter in order to ensure that the thermal performance of the inverter is as designed.

Test procedure:

- The inverter shall be operated by the $I_{t=t0}$ (maximum current defined for the time frame t_0), and the temperature of each part of the inverter shall be recorded after the specified time (t_0) passes.
- The temperature of test inverter shall be measured at the measurement points: electrode part of power semiconductor or specified point of the cooling components closely connected to these parts; inlet and outlet of coolant (additional measurement points can be added).

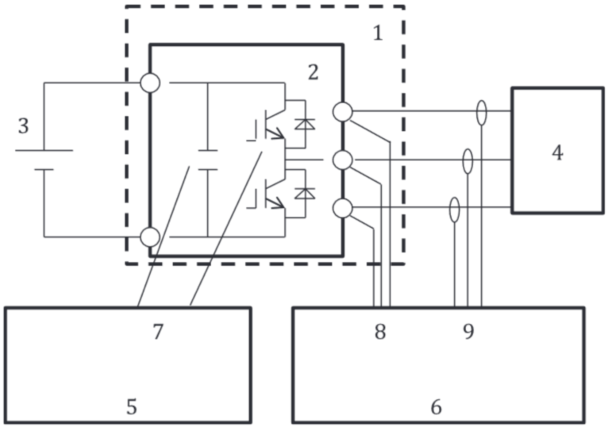


Figure 29 Diagram for temperature rise test of the inverter

where:
1 device under test
2 inverter
3 DC power supply
4 AC load
5 thermometer
6 spectrum analyser/power meter
7 measurement points temperature (in °C)
8 inverter output voltage (in V)
9 inverter output current (in A)

The test conditions are shown in Table 8.

Table 8 Conditions for temperature rise test of the inverter

Test conditions	Values	Remark
Inverter input voltage	Maximum voltage for unlimited operating capability as defined in ISO 21782-1:2023, 3.14.	
Output current	The points as defined in ISO 21782-1:2023, Figure 1 — "a", "b"	
Ambient conditions	Unless otherwise specified, all tests shall be performed at RT of (23 ± 5) °C and with a relative humidity between 25 % to 75 %	
Coolant temperature	Maximum temperature for unlimited operating capability	— In case of liquid cooling — Ethylene glycol and propylene glycol as examples of coolant — If technically feasible, the tests shall be performed at coolant temperature of 65 °C. Otherwise the deviation shall be documented in the test report.
Coolant flow rate	Liquid: Minimum flow rate for unlimited operating capability Air: Minimum flow rate for unlimited operating capability	
Output frequency	Rated frequency (fr) as defined in ISO 21782-1:2023, 3.21.	
Switching frequency	In accordance with the designed frequency	
Operating time	— The operating point "a": 2 s or 10 s — The operating point "b": 1 800 s	

5.2.3 EFFICIENCY MAP

The test is based on an internal TC003 procedure provided by Valeo. The purpose of the test is to measure the high-power inverter efficiency by means of power analyser and the efficiency of the e-axle, calculated from the electrical and mechanical power measurements performed over an entire operating range. Since the e-axle features 2-speed manual gearbox, the efficiency map will be performed for each gear ratio separately.

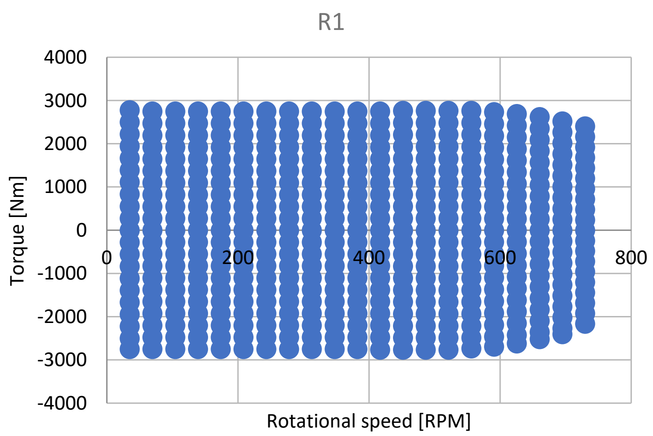


Figure 30 Proposed operating points for transmission ratio 1 (R1)

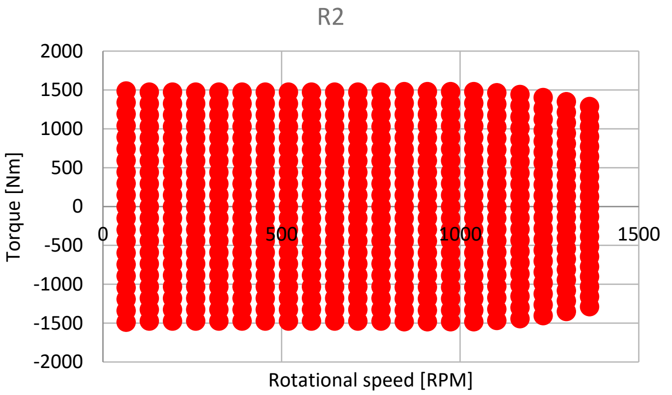


Figure 31 Proposed operating points for transmission ratio 2 (R2)

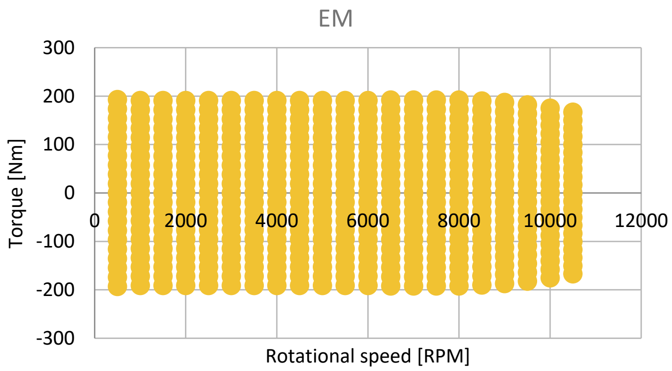


Figure 32 Proposed operating points for electric motor (EM)

5.2.4 EFFICIENCY MEASUREMENT BASED ON DRIVING CYCLE

The test is based on an internal TC004 procedure provided by Valeo. The purpose of the test is to measure the high-power inverter and the e-axle efficiencies in transient conditions over simulated driving cycles. The cycle profile varies for transmission ratio 1 and 2. The analysis of the inverter response to dynamic load will be performed including the assessment of the time delay between the demanded and actual torque and speed values during the acceleration/deceleration events.

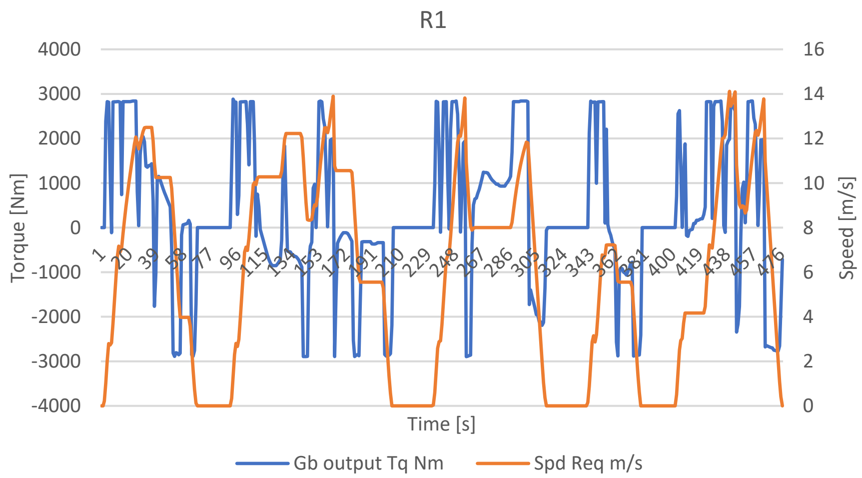


Figure 33 Simulated driving profile for transmission ratio 1 (R1)

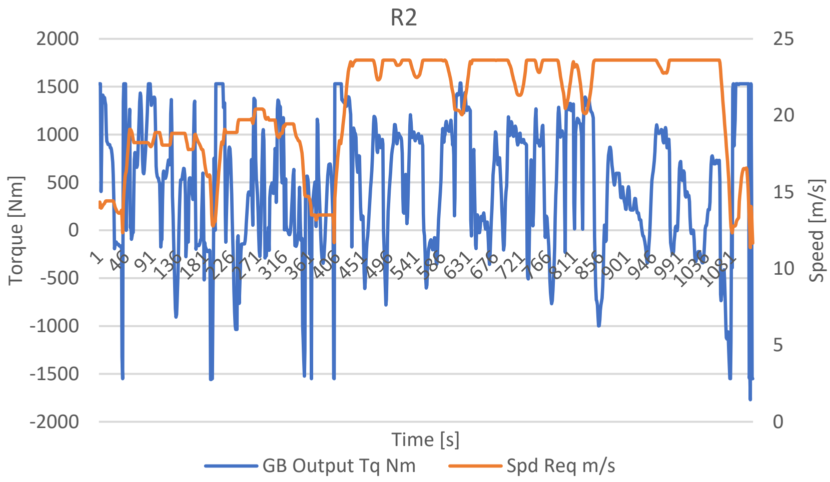


Figure 34 Simulated driving profile for transmission ratio 2 (R2)

5.2.5 MAXIMUM NET POWER AND MAXIMUM 30-MINUTES POWER MEASUREMENT

The test is based on Regulation (EC) no. 85. The purpose of this test is to measure the full load performance to define the points of: maximum net power and maximum 30-minutes power. Subsequently, both maximum power points will be tested for the compliance with the Regulation R85.

5.2.6 OPTIONAL COMPLEMENTARY TESTS

The following test activities are optional and based on a customized procedures aimed to investigate on a selected power inverter and e-axle features:

- Regenerative braking testing:

  The scope of the test is to verify the inverter and e-axle ability to manage energy recuperation during simulated vehicle braking event.
  The test methodology assumes the e-axle operation under motoring/overrun mode (e-axle driven by the dyno) under steady-state and transient operation as a speed ramp: min-> max-> min. Measurement of electrical energy recovered and various energy recuperation strategy/intensity can be tested. Boundary conditions and system limits to be verified.

- Thermal mapping test

  The scope of the test is to measure the inverter performance under various coolant temperature and flow rates.
  The thermal mapping can be performed at selected speed and load steps focusing on boundary conditions and system safety features. The influence of thermal profile on system efficiency can be evaluated.

- E-axle/IMD harmonics analysis

  The scope of the test is to examine the harmonic content in the output waveform, evaluate the HV voltage ripple in the time domain and in the frequency domain.
  Test methodology is based on VW80300 Generated HV voltage ripple

- Fault tolerance

  The scope of the test is to introduce the fault signals (e.g., short circuits) and observe the inverter response.

Test methodology is based on the ISO 16750-2 / LV124 and on VW 80300 standard.
Testing according to ISO 16750-2 / LV124 – LV part of the IMD control unit: overvoltage, superimposed alternating voltage, slow decrease and increase of supply voltage, discontinuities in supply voltage, reset behaviour at voltage drop, short interruptions, pin interruptions/connector interruption, reverse polarity, Short circuit in signal circuit and load circuits.
Test based on the VW 80300 – HV part of the IMD control unit: HV voltage curve parameters, operation within the HV overvoltage/undervoltage range. Functionality check, reset behaviour, occurrence and signalling of incorrect operation to be verified.

- E-axle/IMD noise, vibration and harshness measurement

  The scope of the test is to measure the noise, vibration and harshness performance of the e-axle under operating range with the use of 32 channel analyser triaxial accelerometers: order analysis, spectral maps, peak hold FFT graphs for partial and full load ramp up and ramp down as well as stable speed vibration acquisition. Noise measurements in test beds with microphones, 4 channel SCADAS mobile with spectral and sound quality analysis
  Test methodology includes NVH measurement under steady-state, transient operation at no load/full load points.

- E-axle/IMD thermal imaging camera measurement

  The scope of the test is the assessment of heat distribution inside the high-power inverter and identification of hot spots. Test methodology assumes the heat distribution measurement under steady-state and transient operation for the compliance with the safety limits.

5.2.7 DEMONSTRATION OF THE E-AXLE APPLICATION

As a last part of the test program, the e-axle unit will be fully demonstrated on the test bed as an example powertrain application, including presentation of sensors, software, cloud and CAN bus functionalities.

6 CONCLUSION

This deliverable explains the design, integration, and preliminary validation of the RHODaS high-power hybrid T-type multilevel inverter. Tests were performed at both voltages, 800VDC and 1000VDC.The report details the modular architecture of the converter, the CAD design of the housing, and the integration steps required to assemble the power stages and PCBs. Three identical power stages were manufactured to ensure modularity. The final integration proved more complex and time-consuming than anticipated, particularly in relation to the heatsink preparation and GaN stage isolation. The first GaN inverter highlighted significant mechanical and thermal challenges, which were addressed in the redesign of the second and final inverter. This redesign introduced bottom-cooled GaNs and an additional copper plate soldered to the PCB for improved heat spreading, thereby simplifying integration and enhancing thermal conductivity.

The measured performance of the final prototype demonstrated efficiencies of up to 99% across different load points in both two-level and three-level operation. Thermal measurements indicated GaN temperatures of approximately 82 °C during a 10-minute duration test at 60 A load. Importantly, the prototype achieved a power density of 58.6 kW/l.

Beyond the technical results, this deliverable also defines comprehensive validation scenarios and procedures, aligned with relevant automotive standards (e.g., ISO 21782-3). These procedures, will be applied during the final validation at BOSMAL to ensure full compliance with project requirements.

Although the redesign process introduced a significant delay, it was necessary to achieve a reliable and functional converter prototype. The delivery of the final inverter prototype, despite the time impact, ensures a robust platform for the final validation.