D2.1. INTELLIGENT POWER MODULES WITH INTEGRATED SENSORS AND OTP/OCP CIRCUITS

Reinventing High-performance pOwer converters for heavy-Duty electric trAnSport

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EXECUTIVE SUMMARY

The report focuses on "Intelligent Power Modules with Integrated Sensors and OTP/OCP Circuits." It highlights the design of the power modules, integrated sensors, and fault tolerance algorithms.

The document discusses the selection process for suitable SiC and GaN devices for the converter. The report details the chosen GaN and SiC semiconductors for low and high-power converters, providing their characteristics. Various GaN devices were tested to determine the most appropriate ones.

Additionally, it discusses the functionalities that the gate-driver circuit must possess to protect the converter. Many of these functionalities can be included in commercially available drivers, so the selection process considers the included features. The chosen drivers for both low and high-power converters are specified.

Furthermore, the report outlines the sensors required for implementing the desired functionalities. It presents a study on potential faults that may occur in semiconductors, including their causes and effects. To detect any faults regardless of their origin, a fault detection algorithm based on the aforementioned sensors is developed. The proposed algorithm can identify various semiconductor faults and will serve as a basis for future work on fault localization during WP4.

Overall, the deliverable provides an overview of the design process for power modules, integrated sensors, and fault tolerance algorithms within the RHODaS project. It encompasses the selection of suitable devices, the functionality requirements for drivers, the choice of sensors, and the analysis of potential faults in the system.

LIST OF ACCRONYMS

Acronyms	Definition
ADC	Analog to digital converter
ε	Threshold
EMC	Electromagnetic compatibility
GaN	Gallium nitride
NTC	Negative temperature coefficient thermistor
OC	Open circuit
OVLO	Over-voltage lockout
PCB	Printed circuit board
Rds	Resistance drain source
SC	Short circuit
SiC	Silicon carbide
T_{cx}	Case temperature of transistor *x*
UVLO	Under-voltage lockout
V_{DC}	Total DC bus voltage
Vds	Voltage drain source
V_H	Upper sub-bus voltage
VI+, VI-	Drive inputs
V_L	Lower sub-bus voltage
WBG	Wide band gap

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1 INTRODUCTION

1.1 DESCRIPTION OF THE DOCUMENT AND PURSUE

This report presents the work carried out on the design of the power modules, the integrated sensors and the fault tolerance algorithms. The document outlines the activities performed in this context. Firstly, it describes the selection of the most suitable SiC and GaN devices for the converter, which involved testing with different GaN devices. The report also provides information on the functions and protections required for the SiC and GaN device drivers, as well as the selection of the drivers that offer the desired functionalities. It also explains the selection and definition of the sensors that enable the implementation of the control and protection algorithms of the converter. Lastly, the deliverable includes a study on the fault tolerance of the system, characterizing the possible faults that can occur and the detection methods.

1.2 WPS AND TASKS RELATED WITH THE DELIVERABLE

This deliverable refers to Task 2.1 and Task 2.2 included in WP2: Design of electric and electronics components.

2 POWER MODULES AND DRIVERS

The market offers a variety of SiC and GaN devices. However, very high-power applications, such as the power converter of RHODaS project, have limited options. This section presents the semiconductor devices chosen for the high and low power converters. It also details the selection criteria, and some of the components' functionalities.

2.1 DESCRIPTION OF POSSIBLE SEMICONDUCTORS

The criteria for selecting the semiconductors were detailed in deliverable D1.2. According to these criteria, we chose the potential semiconductors for the low and high-power converters.

The components for the low-power converter are not very critical, as there is a wide variety of WBG transistors available for the required voltage and current levels.

The SiC transistors selected for the low-power converter are the G3R30MT12J from GeneSiC. These transistors meet the specifications defined in the WP1 deliverables, as they have a Vds of 1200 V, a R_{dson} of 30 mΩ and can withstand 60 A at 100 ºC. In addition, they have a TO-263-7 package, which is a very common package that allows these transistors to be easily replaced by other transistors of different models if necessary (for example, they could be replaced with the SCTH70N120G2V-7 manufactured by ST). Figure 2.1 shows the selected SiC MOSFET.

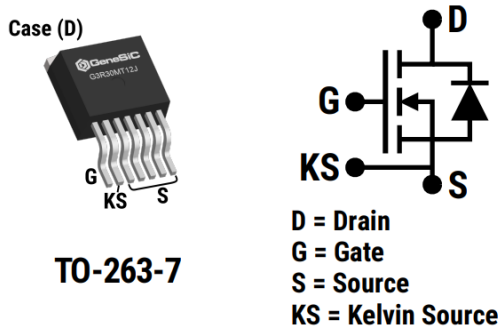

Figure 2.1 Schematic and package outline of the G3R30MT12J

As for the GaN in the low-power converter, the GS66516T model from GaN Systems has been chosen because it is the commercial model that can withstand the highest voltage and current, 650 V and 60 A respectively. In addition, it has a very low R_{ds} of 25 mΩ and allows thermal dissipation on its top side, which minimises the parasitic inductance of the circuit if the PCB is designed appropriately [1]. Figure 2.2 displays the selected GaN transistor.

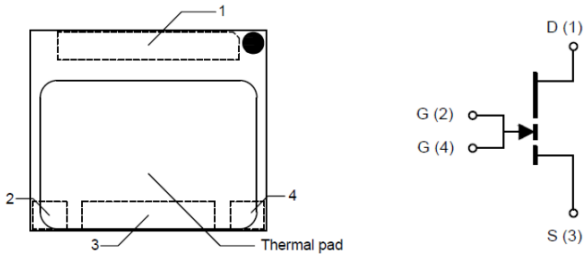

Figure 2.2 Schematic and package outline of the GS66516T

The choice of components for the high-power converter is more challenging, as fewer commercial devices can operate at the voltages and currents required by this converter.

The selected SiC transistors are CAB450M12XM3 from Wolfspeed Cree. According to the datasheet, the selected SiC transistors fulfil the specifications defined in WP1. They have a maximum drain-source voltage of 1200 V, a DC continuous drain current carrying capability of 409 A and an R_{dson} of 2.6 mΩ to 4.6 mΩ, depending on the junction temperature. They have a high-power density footprint and a low inductance design of 6.7 nH. Furthermore, they were available for purchase and additionally they have a practical housing and can thus be easily and uncomplicatedly connected to a heat sink through screw contacts. The layout of the terminals allows for a direct busbar connection and enables a low inductance busbar design. Also, an NTC is included inside the half bridge module to measure the temperature close to the semiconductors. Figure 2.3 shows the schematic and the pin out of the module.

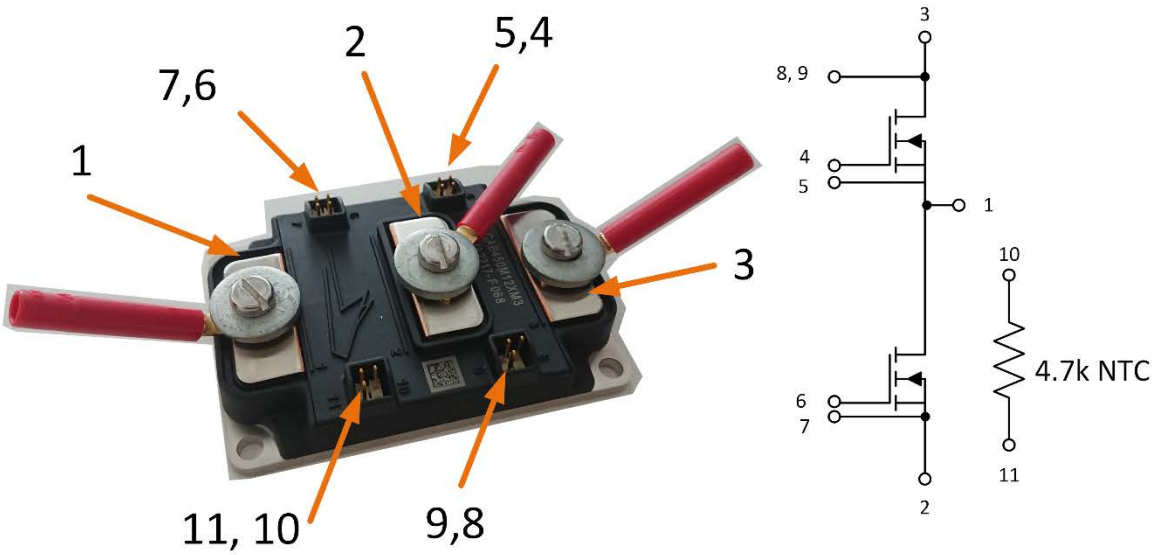

Figure 2.3 Schematic and pin out of the SiC module

The selection of GaN transistors was more challenging because there were no GaN transistors on the market that could meet the high-current capability requirements for a 150 kW inverter. This requirement calls for a current capability of at least 170 Arms, but even higher currents are desirable for the system. Therefore, parallelization of discrete GaNs is required to deliver higher currents. Unfortunately, GaN modules with a common source are not available on the market. Even half-bridge GaN modules are an extreme rarity and not readily available. Originally, GaNs from GaN systems were planned, but the consortium was then provided with preliminary GaNs from Infineon (IGI60F035A1L), which have even better characteristics according to their datasheet. The GaNs have an Rdson of 17 mΩ and are embedded in a thermally enhanced, top-cooled, 12mm x 12mm, lead-free package. What makes these GaNs special, however, is that they have a built-in gate drive. It is planned to parallelize 3 GaNs to reduce the overall R_{dson} to just 5.67 mΩ.

Table 2.1 shows a comparison of the preselected GaNs.

Table 2.1: Preselected GaN transistors

Name and manufacturer	Vds [V]	Id [A]	Rds(on) [mOhm]	Configuration	Integrated driver
GS66516T / GaN Systems	650	60 (@ 25°C) 47 (@100°C)	25 (@25°C) 65 (@150°C)	Single discrete semiconductor	No
GS-065-060-3-T / GaN Systems	650	60 (@ 25°C) 47 (@100°C)	25 (@25°C) 65 (@150°C)	Single discrete semiconductor	No
GS-065-060-5-T-A / GaN Systems	650	60 (@ 25°C) 41 (@100°C)	25 (@25°C) 65 (@150°C)	Single discrete semiconductor	No
GS-065-150-1-D2 / GaN Systems	650	150	10	Discrete die	No
Amotech Half-bridge module	650	100 (Tc = 25°C)	10	Half-bridge module	Yes
IGI60F017A1L / Infineon	600 (700V transient immunity)	104 (Tc = 125°C)	17 – 21 (@25°C)	Single semiconductor	Yes

As shown in Table 2.1 the GaN half-bridge module from Amotech offers a lower R_{dson} compared to the IGI60F017A1L from Infineon. However, in project Rhodas a single semiconductor configuration is preferred because the GaN semiconductors are used in a common source configuration and not as a half-bridge. When using the Amotech half bridge module two modules for each T-type leg must be applied, whereby only one GaN in each half-bridge is used. This would require too much space and resources. However, by using three IGI60F017A1L from Infineon in parallel an even lower R_{dson} (5.67 mΩ) could be achieved. Furthermore, the IGI60F017A1L from Infineon has a 12x12 mm S-Trace package which already includes an integrated driver which saves additional space and costs.

2.2 EXPERIMENTS AND SELECTION CRITERIA

This section presents the simulations and experiments that we performed to test the proper functioning of the semiconductors that we selected for the high-power converter.

2.2.1 SIMULATIONS

Based on the selected semiconductors, LTspice simulations were performed to demonstrate the functionality of a T-type multilevel converter with both SiC and GaN. For the SiC modules, the models of the semiconductors (CAB450M12XM3) were used.

A comparison of the SiC modules in half-bridge switching mode with the measured double-pulse test showed that the model was reliable. For the GaNs, the GaN systems semiconductor model (GS66516T) was used, but the simulation will be performed also with the infineon GaNs (IGI60F017A1L), as soon, as a reliable model is available. For simplicity and to speed up the simulation, GaNs were not yet connected in parallel. Parasitic effects were included in the simulation within the DC link capacitances, with a series inductance of 40 nH added to create realistic conditions. Other parasitic effects were neglected to speed up the simulation. The dc-link voltage was set at 900 V and the load current at 50 A to avoid exceeding the allowable current limit of the GaNs. Figure 2.4 shows the simulated system.

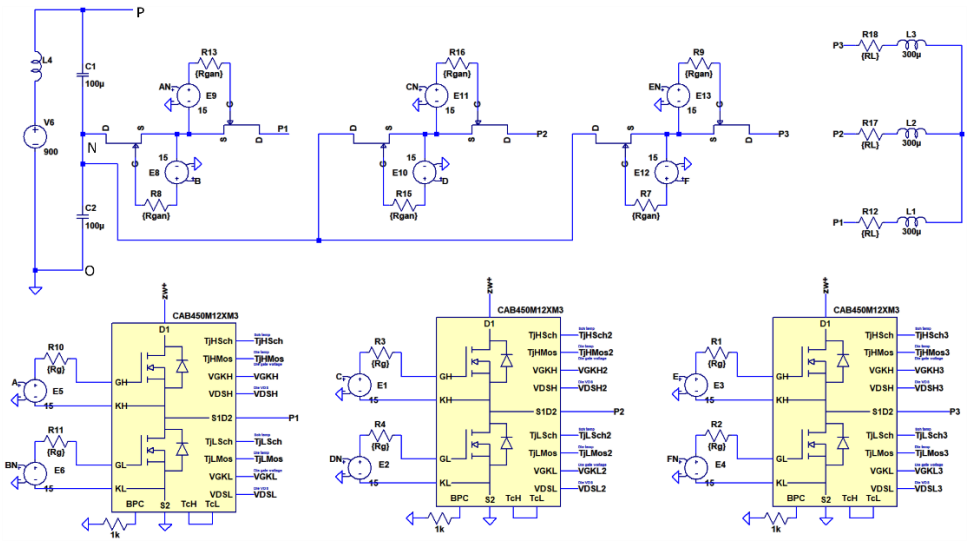

Figure 2.4 Simulation setup of the three T-Type phases with the SiC modules CAB450M12XM3 and GaNs

Figure 2.5 shows the simulation results obtained with the described simulation setup. The switching frequency was set to 100 kHz. The output current is shown in the upper part of the figure, where a sinusoidal current smoothed due to the load inductance can be seen. The middle part of the figure shows the voltages on the GaNs branches, where they alternate between +450 V and -450 V with voltage peaks. It will come down to these voltage spikes as to what DC link voltage the GaNs will still survive, since they are specified for 600V and transients up to 700 V are allowed. Depending on the parasitic effects, overvoltages will occur to some degree. For the simulation a carrier-based sine pulse width modulation was used. The lower part of the figure shows the line-to-line voltages U_{P12}, U_{P23} and U_{P31}. All in all, the simulation results obtained confirm that the selected semiconductors are suitable for the multilevel converter application and reinforce the selection for the semiconductors.

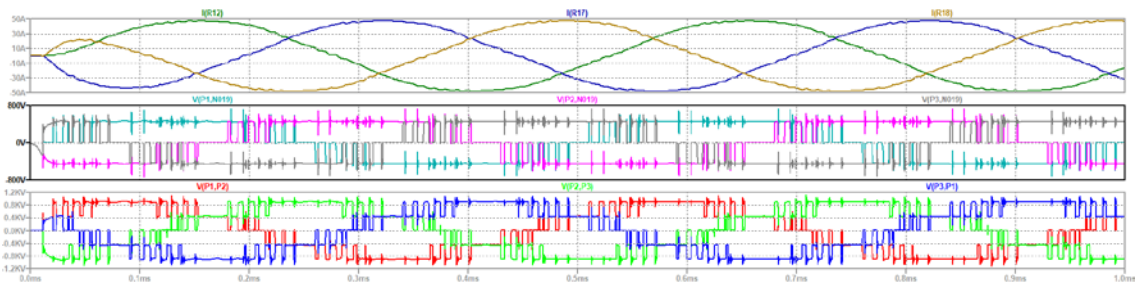

Figure 2.5 Simulation results showing the phase currents ($I_{1,2,3}$), line-to-neutral voltages (U_{P1N}, U_{P2N}, U_{P3N}) and the line-to-line voltages (U_{P12}, U_{P23}, U_{P31}) with the SiC Modules combined with GaN semicoductors.

2.2.2 EXPERIMENTS

Double pulse tests were carried out with the SiC power module CAB450M12XM3. During these tests, the basic operation could be demonstrated as shown in Figure 2.6. The test setup consisted of a SiC half-bridge with a control board, as also shown in Figure 3.3, and additionally an external load inductance of about 50 µH. The goal of this test was to show the switching behaviour and general functionality of the SiC module under live conditions. Figure 2.6 shows the high side gate (HS gate), the low side gate (LS gate), the output voltage (output), the inductive load current and the input current. Unfortunately, the experimental setup was not optimal because the experimental setup produced a high DC link inductance because the DC link capacitance was connected too far away with a large loop, since the optimal DC link setup was not yet built. This resulted in a lot of ringing during the measurements and a high overvoltage. With a DC link voltage of 800 V, a maximum voltage of 1200 V was already reached. This showed once again how important a low inductive DC link capacitance is. Therefore, it was decided to design our own DC link board with connections that are low inductive and optimized for our setup. It is expected to reach significant less ringing with an optimized setup and reach the planned DC Link voltages. Nevertheless, the measurements showed that the functionality of the modules is given, and some optimizations will lead to a reliable switching action.

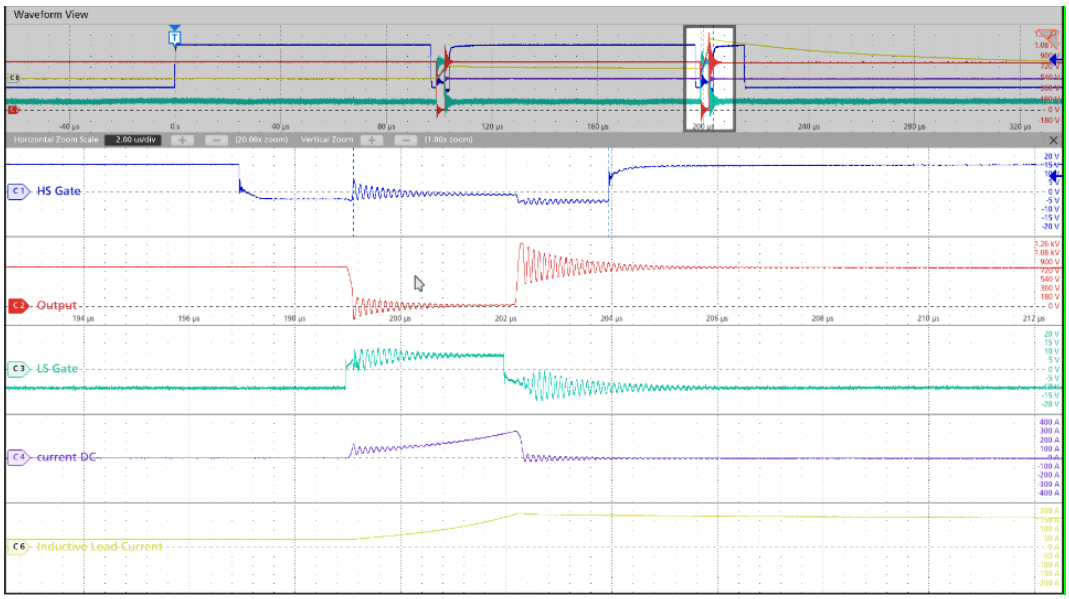

Figure 2.6 Measurement results of the SiC Halfbridge (CAB450M12XM3)

3 DRIVERS AND FUNCTIONALITIES

WBG transistors need drivers that can handle high switching frequencies and deliver the required voltage levels at the gate of SiC or GaN. GaN transistors are particularly challenging as they are very susceptible to voltage spikes at the gate and to the parasitic inductance of the gate-driver circuit [2]–[6]. Hence, it is essential to specify what functionalities and protections the drivers should have. This way, reliable drivers that include the specified functionalities can be selected to ensure the proper switching of the devices and minimise or prevent failures.

This section outlines the various functionalities that have been specified for the drivers of the WBG semiconductors. Moreover, the selected drivers are described, and the functions and protections of each one are discussed.

3.1 FUNCTIONALITIES

This subsection explains the main features of the gate driver circuit for the T-type converter. These functionalities can be achieved either with the chosen driver or with external sensors. Note that some of these functions were briefly defined in D1.2.

3.1.1 DIFFERENTIAL INPUT

Some drivers have two drive inputs (VI+ and VI−) to control the transistor gate drive signals. With the VI− pin low, the VI+ pin accepts positive logic. If VI+ is kept high, the VI− pin accepts negative logic. Table 3.1 shows the truth table of the drivers. Notice that the output is high only if VI+ is high and VI- is low. Therefore, we can use both inputs to protect the transistor from noise, such as crosstalk. The procedure is as follows: one input (VI+) receives the PWM signal from the transistor itself. The other pin (VI-) receives the PWM signal from the complementary transistor. Thus, the transistor will only activate when its signal is positive and the complementary signal is negative. This method prevents false switching that can cause additional losses and even the destruction of the transistor.

Table 3.1: Truth table of a driver with differential input.

VI+	VI-	OUTPUT
Don’t care	Low	Low
Low	High	High
High	Don’t care	Low

3.1.2 MILLER CLAMP

Drivers may have an internal Miller clamp to reduce voltage spikes on the gate. These spikes are caused by the Miller capacitance during the transistor's shutoff. When the input gate signal asks the transistor to be turned off, the Miller clamp MOSFET is initially off. The clamp is activated at a certain voltage, typically 2 V, on the gate drive output's falling edge. When the clamp is active, it creates a second low-impedance current path for the gate current to follow. The Miller clamp switch stays triggered until the input drive signal switches from low to high.

3.1.3 UVLO & OVLO

Most drivers have under-voltage lockout (UVLO) protections for both the primary and secondary sides of the device. If either voltage falls below the UVLO threshold, the driver outputs a low signal, i.e., the transistor is turned off. The UVLO detection has some hysteresis to allow for small voltage source fluctuations. Moreover, some drivers have an over-voltage lockout (OVLO). The driver outputs a low signal when the voltage rises above the OVLO threshold.

3.1.4 SATURATION & OVERCURRENT

There are drivers with protections against saturation and overcurrent. If saturation is detected, the driver shuts down the gate drive until a RESET signal arrives. Furthermore, component failures may occur with the circuitry connected to the transistor linked to the driver, such as shorts in the motor windings or shorts to power buses. The resulting excess of current flow makes the semiconductor exit saturation. In this scenario, the driver enters the failure state and turns the transistor off until a RESET signal arrives.

3.1.5 THERMAL SHUTDOWN

Some drivers also have an internal thermal shutdown. The gate driver is turned off when the internal temperature of the driver goes above a certain value. This state persists until the internal temperature falls below a threshold. Alternatively, temperature sensors can be incorporated near the transistors to monitor their temperature and open them in case of extremely high temperatures.

3.2 DRIVERS

The drivers used in the RHODAS have been chosen for their robustness and properties. In the low-power converter, GaN e-HEMTs use the driver ADUM4121ARIZ (Figure 3.1), while SiC MOSFETs use the driver ADUM4135BRWZ (Figure 3.2). Both drivers are fast and have several interesting features related to converter protection and fault detection.

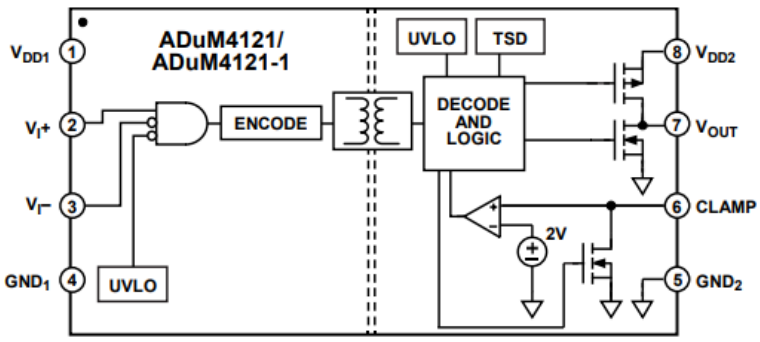

Figure 3.1 ADUM4121ARIZ functional block diagram

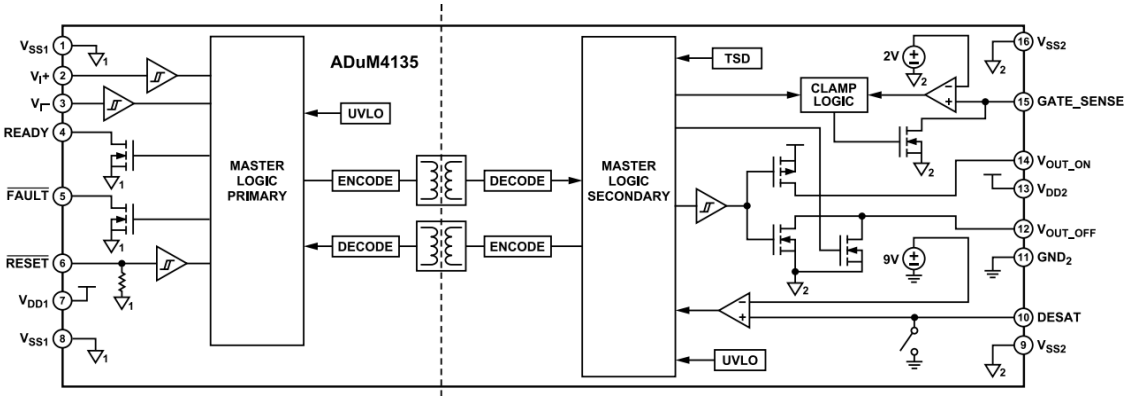

Figure 3.2 ADUM4135BRWZ functional block diagram

Both drivers share some of the functionalities described above. For example, both drivers have a differential input to prevent crosstalk and false switching of the transistor. Furthermore, both drivers have a miller clamp to avoid voltage spikes at the gate of the transistors. In this case, the clamp is triggered at 2 V. Both drivers are isolated and have UVLO on the primary and secondary side. However, they lack OVLO. The two drivers also feature a thermal shutdown that switches off the driver and opens the transistor when the temperature exceeds 155 ºC and switches it back on when the temperature drops below 125 or 135 ºC, depending on the driver. Lastly, only the SiC driver, the ADUM4135BRWZ, has protections against saturation and overcurrent.

Table 3.2 shows the properties of the drivers selected for the low-power converter. As shown, the drivers satisfy most of the functionalities specified earlier.

Table 3.2: Low-power converter driver functionalities

Function	ADUM4121ARIZ	ADUM4135BRWZ
Differential input	Yes	Yes
Miller clamp	Yes	Yes
UVLO & OVLO	UVLO	UVLO
Saturation & Overcurrent	No	Yes
Thermal shutdown	Yes	Yes

For the high-power converter, matching drivers were also available from Wolfspeed Cree (CGD12HBXMP). They were specifically designed for the half-bridge and fit perfectly onto the modules. The driver board includes an ADuM4135 isolated gate driver from Analog Devices. The selected driver offers a peak output current of 4.61A when using a 2 mΩ gate resistance. Figure 3.3 shows the driver PCB, the control PCB, and the function block diagram of the first test setup.

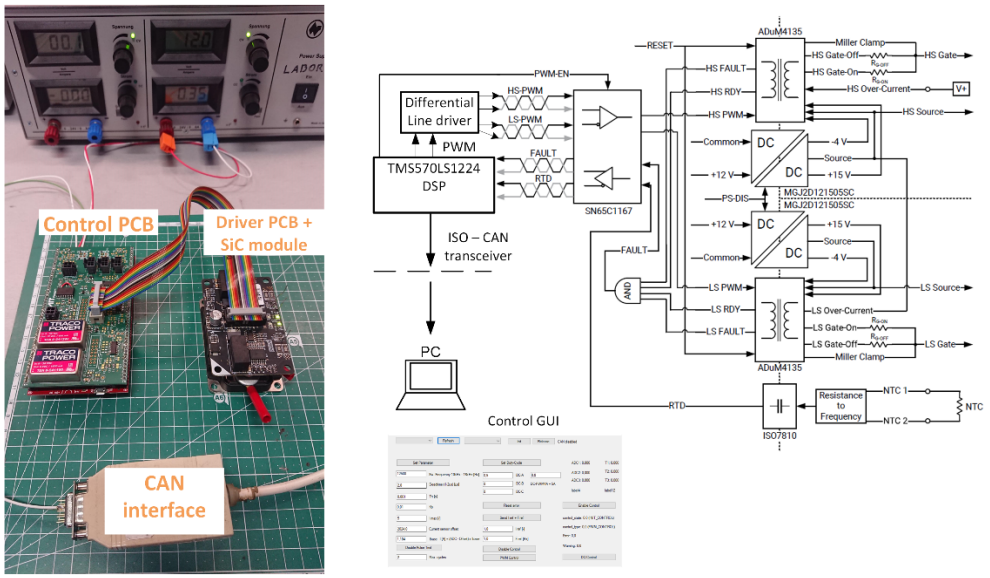

Figure 3.3 First test setup including the control PCB and the driver PCB with the SiC module

The ADuM4135 provides an OVLO and a UVLO, where the circuit detects when the output rails of the driver supply fall outside the safe operating conditions of the gate driver. Another safety feature is overcurrent protection. The overcurrent protection circuit measures the drain-source voltage, and the fault will indicate if this voltage has exceeded a safe current limit. When a fault has occurred, the corresponding gate driver channel will be disabled. Figure 3.4 shows parts of the schematic and the overcurrent protection of the low side driver.

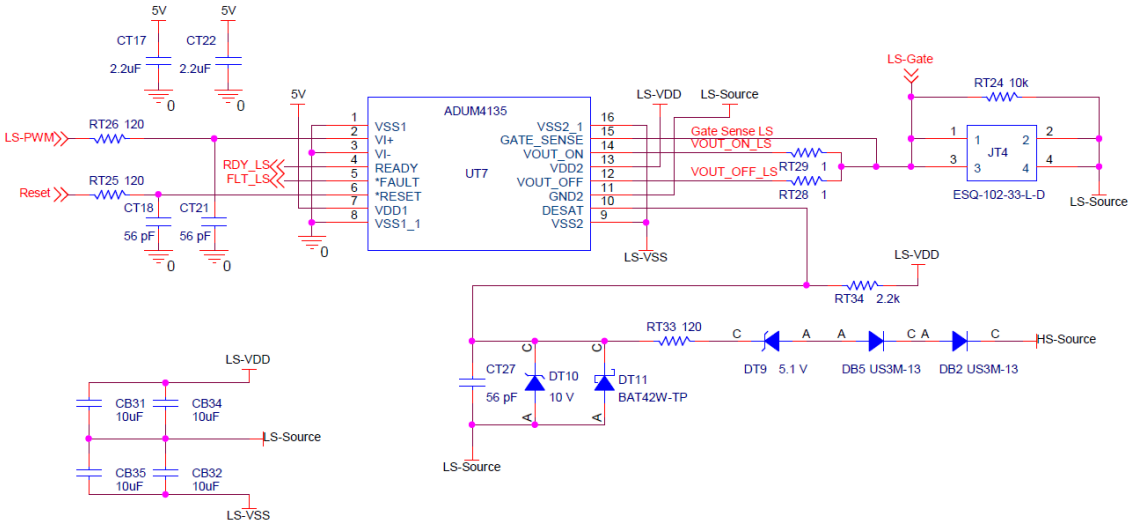

Figure 3.4 Low side driver schematic with adjustable desaturation circuit

The internal desaturation comparator threshold voltage is 9 V. The threshold current can be adjusted by choosing an alternative Zener diode (DT9). With a 5.1 V Zener diode the over-current trip point is at approximately 1000 A (@25°C). Moreover, the driver has shoot-through protection, preventing the half-bridge from switching to a short circuit. The driver also has a differential PWM input, that prevents false turn-on due to possible EMC interference. Temperature feedback is also provided by the driver by being connected to the NTC that is built into the module. The driver converts the NTC resistance value into a 50% duty cycle square wave with varying frequency for further

processing. The temperature measured by the NTC differs significantly from the junction temperature of the SiC MOSFETs and is not suitable as a junction temperature measurement.

The Infineon (IGI60F035A1L) GaNs have an integrated gate driver that enhances the switching performance and provides an optimal gate loop for each device. The gate driver only needs an isolated PWM signal and a gate voltage supply as inputs. The gate resistors are placed outside the transistor package, where the switching speed can be fine-tuned. The only protection function that the GaN driver offers is a UVLO to avoid turning on the GaN below a certain threshold voltage level.

Table 3.3 shows the properties of the drivers selected for the high-power converter. As shown, the drivers satisfy most of the functionalities specified earlier.

Table 3.3: High-power converter driver functionalities

Function	CGD12HBXMP	IGI60F035A1L
Differential input	Yes	No
Miller clamp	No	No
UVLO & OVLO	Yes	UVLO
Saturation & Overcurrent	Yes	No
Thermal shutdown	No	No

4 CRITICAL SENSORS

There are a series of critical sensors required to implement all the functionalities in the transistors and their protections. Fortunately, as mentioned in the previous section, some of these functions are implemented with the drivers themselves. However, other functions require additional sensors to be performed correctly. The required sensors are as follows:

- **Temperature sensors**: These sensors allow us to measure the temperature of different semiconductors and modules. Monitoring the temperatures of different components allows us to detect abnormal temperatures and, therefore, semiconductor failures.
- **Voltage sensors**: Voltage sensors allow us to monitor the system voltages. On the one hand, they allow us to measure the voltages on the DC bus and easily detect if there are short circuits in the semiconductors or failures in the capacitors. On the other hand, they allow us to measure the output voltages of the converter and thus verify if the converter is switching correctly.
- **Current sensors**: These sensors measure the output currents of the converter, which allows us to detect overcurrents, change the operation mode of the converter from two-level to three-level or vice versa, and close the control loop.

Below are the different sensors chosen to be implemented in the power converters, their characteristics, and their location.

The low-power converter incorporates NTC thermistors (NTCLE400 manufactured by Vishay) connected to a 10 kΩ resistor. These sensors provide a different voltage level depending on the temperature they measure. Consequently, by reading this voltage, we can know the temperature of the semiconductors. In the case of the low-power converter, an NTC sensor will be placed next to each transistor to measure the temperature of its encapsulation. It should be noted that the encapsulation temperature will always be lower than that of the junction, so this difference must be taken into account when estimating the temperature inside the semiconductor.

In the high-power converter, each SiC half-bridge module (CAB450M12XM3) includes a 4.7 kΩ NTC temperature sensor. The driver board (CGD12HBXMP) converts the NTC resistance value into a 50% duty cycle square wave with varying frequency depending on the temperature for further processing. To monitor the GaN temperature multiple 10 kΩ NTC SMD temperature sensors will be placed close to the GaN semiconductors to detect an over-temperature failure. The temperature sensors for the GaNs are directly connected to the control PCB. To save ADC channels a multiplexer was included to the control PCB.

The current sensor incorporated in the low-power converter is the LA-25-NP. There is a current sensor in each phase to read the output currents. This sensor, manufactured by LEM, allows reading currents of up to 25 A and has two peculiarities that make it interesting. Firstly, it is an isolated sensor, which avoids noise propagation from primary to secondary. Secondly, the output of the sensor is current, not voltage. Current is much less susceptible to EMI than voltage, so readings will be more reliable. However, many analogue-to-digital converters read voltage, and this implies that additional circuitry will be necessary to transform the output current of the sensor into a range of voltages. Figure 4.1 shows the current sensor scheme provided by its manufacturer.

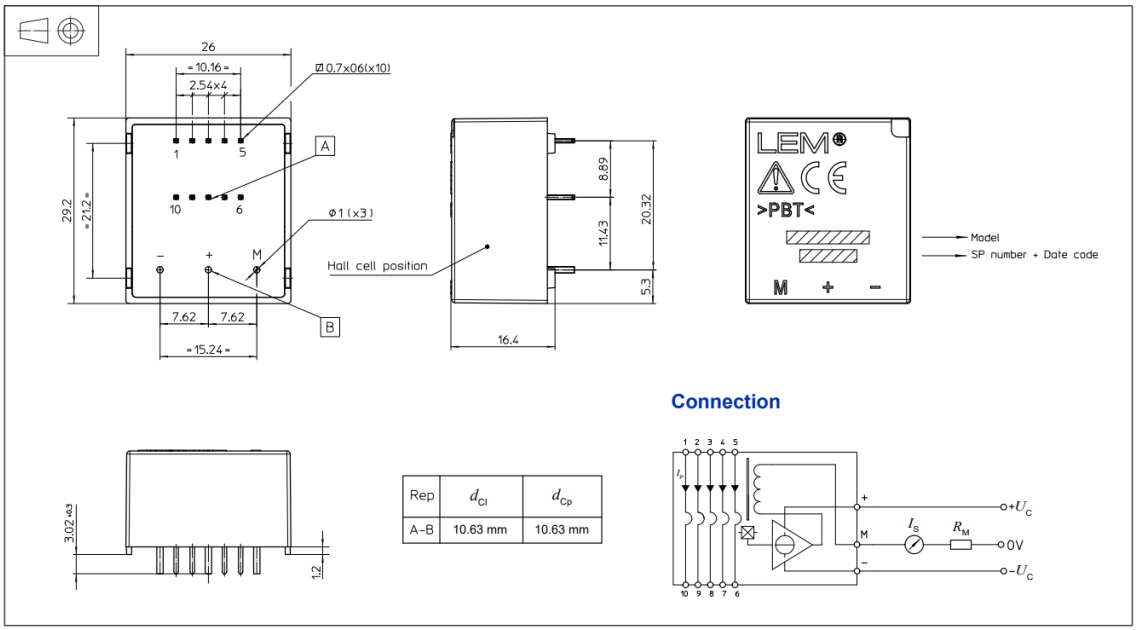

Figure 4.1 Schematic of the current sensor LA-25-NP

The control platform of the high-power inverter will offer four current sensor front-ends for closed loop Hall effect sensors like the LF 306-S or LF 505-S from LEM. These sensors offer high accuracy and bandwidth. The measurement range can be selected up to 500 A (peak). Figure 4.2 shows the front-end design for the current sensor inputs.

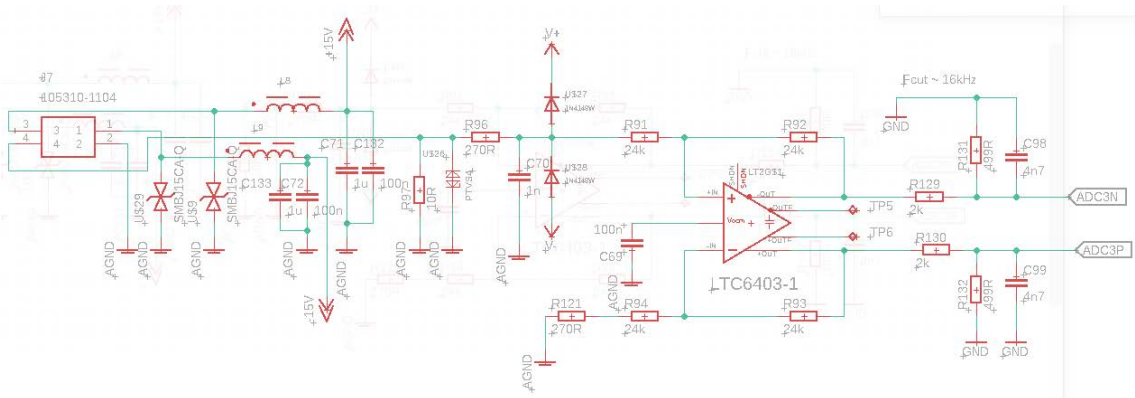

Figure 4.2 Current sensor front-end design.

In the low-power converter, the LV 25-P sensor is used to read the different voltages of the system. There is a voltage sensor to read the output voltage and others to measure the DC semi-bus voltages. These sensors are also manufactured by LEM and have similar characteristics to the LA-25-NP current sensors: they are isolated sensors and their output is current. In addition, they allow reading voltages of up to 500 V, which makes them ideal for the low-power converter. Figure 4.3 shows the voltage sensor scheme.

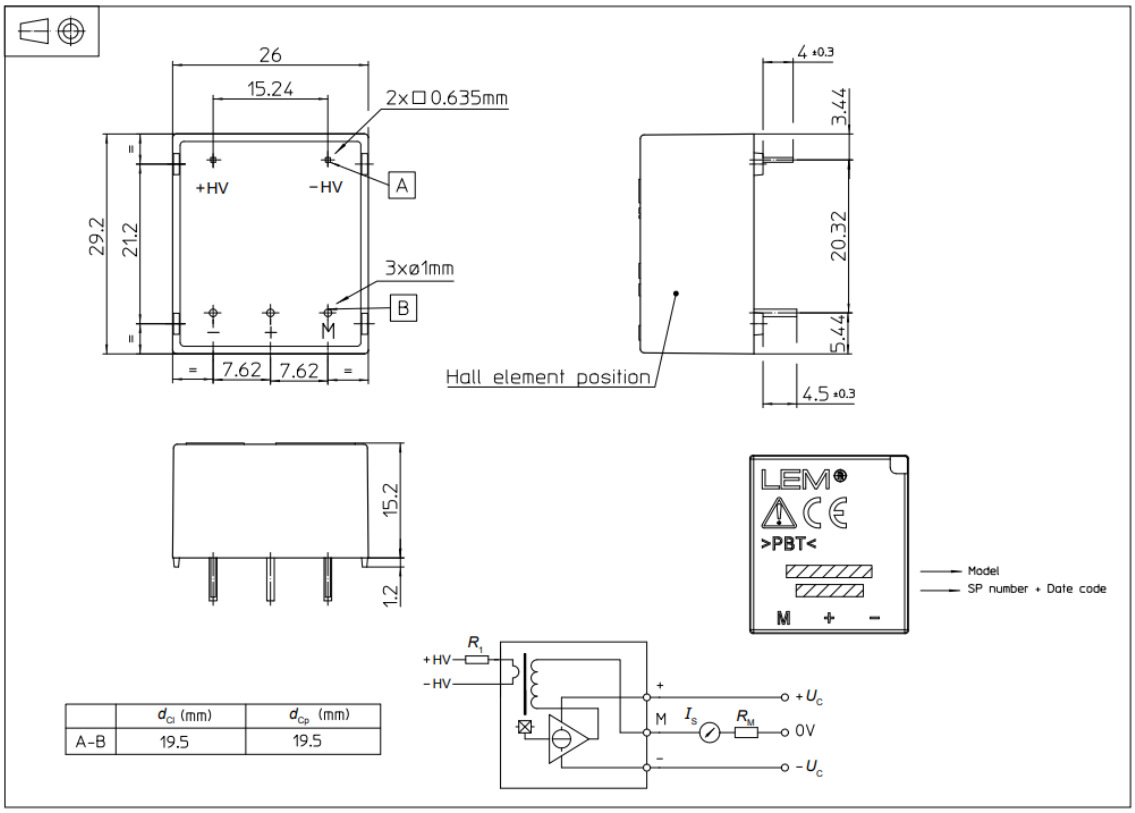

Figure 4.3 Schematic of the voltage sensor LV 25-P

However, the total DC bus voltage is higher than the voltage sensors can handle, 800 V on the low-power converter. Therefore, another sensor model is needed to measure the total voltage. The chosen sensor is the DVC 1000-P from LEM, which has similar characteristics to the ancillary sensors. However, the sensor output is a voltage signal and it can measure voltages up to 1000 V. Figure 4.4 shows the schematic of the voltage sensor.

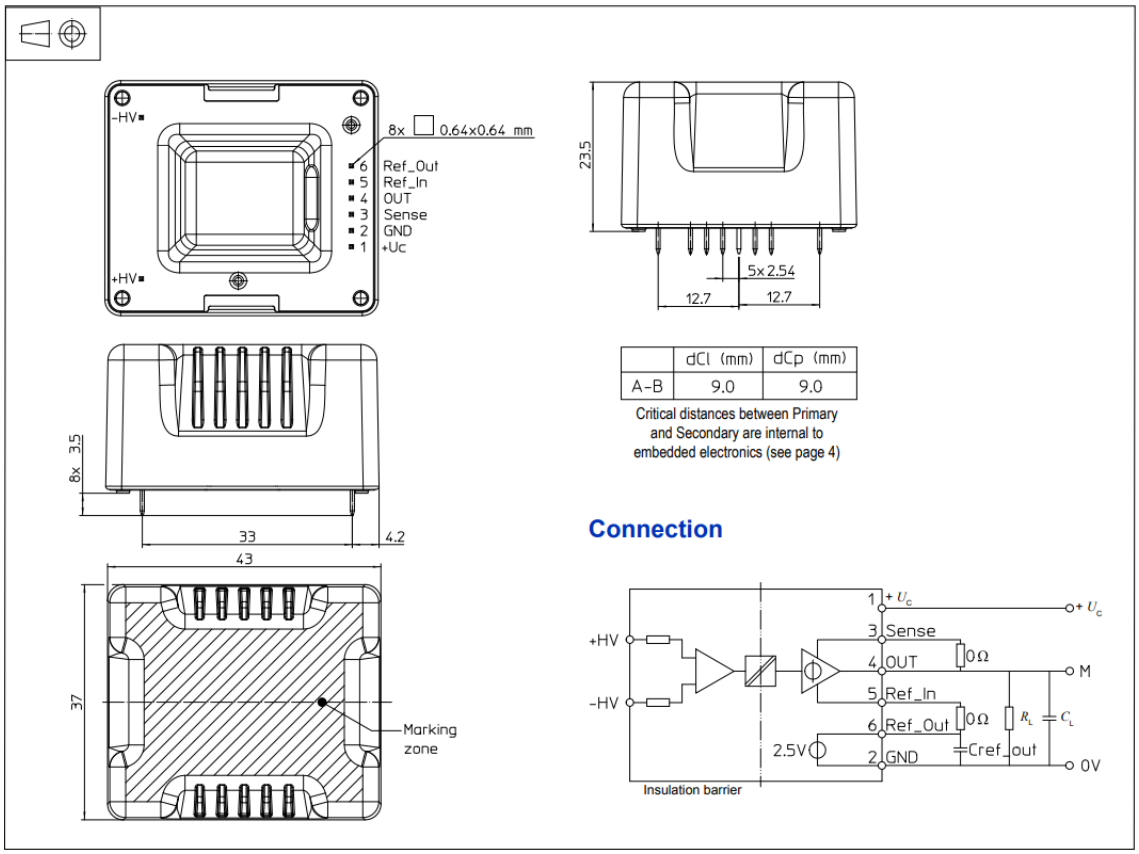

Figure 4.4 Schematic of the voltage transducer DCV 1000-P

The high-power converter will measure the voltages U_{DC1} and U_{DC2} as shown in Figure 4.5. To measure these voltages, DC voltage isolation sensors with integrated sigma-delta ADCs (ACPL-C87BT-500E or ACPL-782T-300E) will be placed close to the DC-link bus bar to detect unbalance or overvoltage conditions.

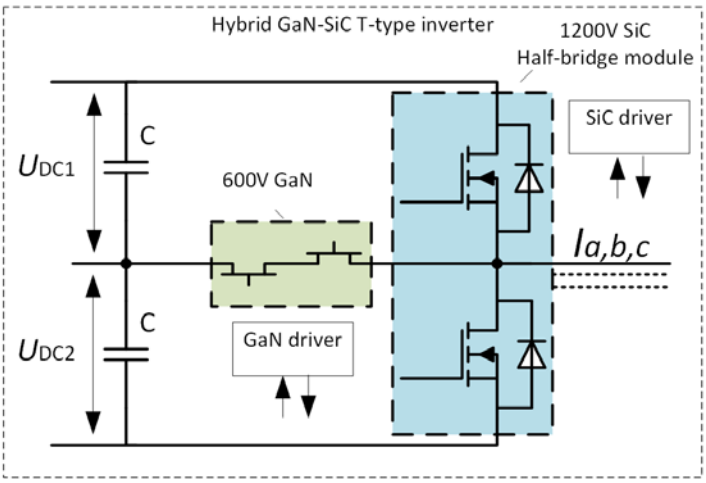

Figure 4.5 U_{DC1} and U_{DC2} will be measured to detect unbalance or overvoltage conditions.

Moreover, the control board of the high-power converter includes a resolver interface based on the AD2S1200 resolver-to-digital converter with an excitation frequency of 10 kHz and ~7 VRMS. The AD2S1200 is connected to the SoC controller over SPI or over a 12-bit parallel interface. The AD2S1200 also provides an encoder emulation which is also connected to the main SoC controller.

5 SWITCH FAULT ANALYSIS

In a T-type converter, it is important to understand how and why the semiconductors may fail more than in other converter topologies, due to the high number of semiconductors it requires. The most common fault in power converters is the capacitor fault, followed by the semiconductor fault. Semiconductors can fail in open circuit (OC) or short circuit (SC), although the former is more frequent [7], [8]. In addition, transistors can partially fail, i.e., they do not break completely but their performance is affected, their switching is more lossy and consequently the transistor heats up. Moreover, other components, such as inductors or sensors, can also fail [7].

Power transistors can fail for various reasons, such as mechanical, thermal, electrical stress, or electromagnetic radiation. Some causes of failure are the following [9]:

- **Overvoltage:** if the voltage that the transistor sees exceeds its maximum peak voltage, this can cause it to break. This overvoltage can happen due to a failure in the DC bus or the parasitic inductance of the circuit, which produces voltage spikes during switching (ringing). To minimise this risk, the converter should be designed to reduce the parasitic inductance of the power loop and monitor the DC bus voltages.
- **Overcurrent:** similar to overvoltage. An excessive current flowing through the transistor can cause it to overheat and fail. Some drivers have protections against this type of failure.
- **Short – circuits:** Automotive motor drives operate in harsh environments in which high temperature, mechanical overload, short-circuits in motor windings, problems with wiring harnesses and other critical contingencies such as electromagnetic interference or a malfunction in the controller can occur. These events result in large **overcurrent levels and even short-circuits** flowing in the motor drive power circuits, which destroy the device in the order of microseconds. Current measurement or desaturation detection is typically implemented in many drivers for overcurrent and short-circuit device protection.
- **Thermal stress:** an excessive temperature in the transistor can reduce its life expectancy and even cause damage and failure of the semiconductor. This overtemperature can be caused by many factors, such as bad soldering, a poor thermal dissipation system, overcurrents, a transistor that does not switch well due to a manufacturing defect or the converter working at too much power for too long. Temperature probes can be used to monitor this failure near the transistors or inside the modules used. Some commercial modules already have NTC probes to measure the temperature easily.
- **Electromagnetic interference:** electromagnetic interference can cause false switching in the transistors and, therefore, short circuits and destruction of the converter. There are several ways to mitigate this, such as designing the converter to minimise the parasitic inductance of the power loop and gate-driver circuit, using drivers with differential inputs to prevent noise in the PWM signals from affecting switching, and sending PWM signals to the driver in differential mode or using systems with noise robustness such as optical fibre.
- **Mechanical stress:** environmental stress such as vibrations, temperature or humidity can damage the physical structure of the transistor or cause false electrical contacts. To avoid this, the converter should be designed taking into account the final conditions of use and environmental factors of the places where IMD use is planned.

Moreover, to ensure the reliability of the power converter, electronic soldering must be done with high quality. Otherwise, many problems may arise, such as faulty contacts, voltage drops, performance degradation and other issues that compromise the functionality.

Several factors affect the quality of electronic soldering, such as: the material choice, the surface preparation, the temperature control and the soldering process control. To verify that the soldering is done correctly and does not cause any component failures, various methods and protocols can be applied:

- **Visual inspection:** This is a simple technique that involves checking the soldering for any defects or quality issues by looking at it.
- **X-ray inspection:** This is a non-destructive technique that can reveal any hidden defects in the soldering, such as porosity, contamination or other irregularities.
- **Ultrasonic inspection:** This is another non-destructive technique that uses ultrasonic waves to scan the soldering and detect any flaws.
- **Metallurgical analysis:** This is a technique that assesses the quality of the solder metal by analysing its composition and properties. It ensures that the materials used for soldering are suitable and free of any impurities or anomalies.

As discussed earlier, transistors can fail in either OC or SC modes. It is important to analyse how the transistor behaves under different stress conditions, such as overvoltage or overcurrent. Therefore, we will build and test additional phases of the low-power converter under extreme scenarios to investigate the transistor failure modes and the effectiveness of the protection mechanisms. The details of the experiments with the low-power converter will be provided in deliverable D2.4.

5.1 FAULT DETECTION ALGORITHM

This subsection introduces the fault detection algorithm for the power converter of the RHODaS project. This algorithm is a component of the fault tolerance algorithm that will be fully developed in WP4. However, the algorithm presented in this deliverable is an integral part of the final algorithm and will serve as a foundation for developing the rest of the algorithm.

The proposed algorithm measures various signals from the power converter and verifies if they are within normal ranges or if they deviate significantly from the expected values. Subsequently, a fault localization algorithm will be integrated with the current one. The localization component is an algorithm that identifies which part of the converter is malfunctioning. The combined detection and localization algorithms will constitute the complete fault tolerance algorithm for the converter of the RHODaS project.

The proposed detection algorithm uses three methods to detect faults:

- **Temperatures:** Temperature sensors are used to monitor the temperatures of the different semiconductors. Monitoring temperatures, in addition to protecting the converter, allows for detecting anomalous temperatures. Hence, if one of the transistors has a much higher or lower temperature than the rest, it may be failing. Notice that monitoring transistors' temperatures allows not only to detect but also to locate the faulty semiconductor.

- **DC bus voltages:** T-type converters have a split DC bus to connect the central branch to the midpoint of the bus and thus generate the “0” voltage level. Usually, in these converters the upper and lower sub-buses are measured to verify the state of charge of the bus and see if it is balanced. The proposed converter uses three voltage sensors to measure the voltages in the DC bus: one for the upper sub-bus, one for the lower sub-bus and one for the total bus voltage. It must always be fulfilled that:

$$\varepsilon > |V_{DC} - (V_H + V_L)| \quad (1),$$

where ε is a certain threshold value, V_{DC} is the total bus voltage, V_H is the upper sub-bus voltage, and V_L is the lower sub-bus voltage. Ideally, the threshold should be zero but it may not be due to non-idealities in the measurement, noise and sensor accuracy among other parameters. Therefore, an acceptable threshold value must be determined experimentally.

There is always a delay between a fault and its detection. To minimize this response time alarms are configured for the previous voltage sensors. It is an indicator of fault that a voltage sensor detects a value too high (higher than V_{DC} or $V_{DC}/2$) or too low (close to 0). These faults may be due to a fault in the capacitors or the sensor itself, although normally when a sensor fails its reading is a constant zero [7]. These faults can also occur in case of a short circuit in the transistor.

- **Output voltages:** Each phase of the converter can produce three different output voltage values: Vdc/2, -Vdc/2 and 0. The output voltage depends on the transistors' state, as shown in Table 5.1.

Table 5.1: Possible states of the T-type converter.

S_{x1}	S_{x2} = not(S_{x4})	S_{x3} = not(S_{x1})	S_{x4}	V_x
0	0	0	0	---
0	1	1	0	0
0	0	1	1	$-V_{DC}/2$
1	1	0	0	$+V_{DC}/2$
1	0	0	1	Not possible

The switches S_{x2} and S_{x3} always have an opposite state to S_{x1} and S_{x4}, respectively. Therefore, we can determine the output voltage of a phase of the converter by simply looking at the state of S_{x1} and S_{x4}. The equation that defines the theoretical output voltage of phase "x" of the converter is:

$$V_x^* = S_{x1} \cdot \frac{V_{DC}}{2} - S_{x4} \cdot \frac{V_{DC}}{2} \quad (2),$$

where S_{xi} can take the values 0 when the transistor is open, and 1 when it is closed.

After calculating the theoretical output voltage, it is compared with the actual voltage according to

$$\varepsilon > |V_x^* - V_x| \quad (3),$$

As shown by (3), the error must be lower than a certain threshold, which must be determined experimentally. If the error is higher than that threshold, there is a fault in the converter.

An additional time requirement can be implemented to declare a fault. The output of the previous comparison, i.e., ε, enters a counter. When this signal is 1, the value of the counter increases. The value of the counter keeps increasing until the output of the comparison is 0, and then it resets. If the value of the counter is higher than another threshold, "*N*", a fault in the converter is declared. Figure 5.1 shows the schematic of the fault detection algorithm for the output voltages. This scheme can be extrapolated for the rest of the faults.

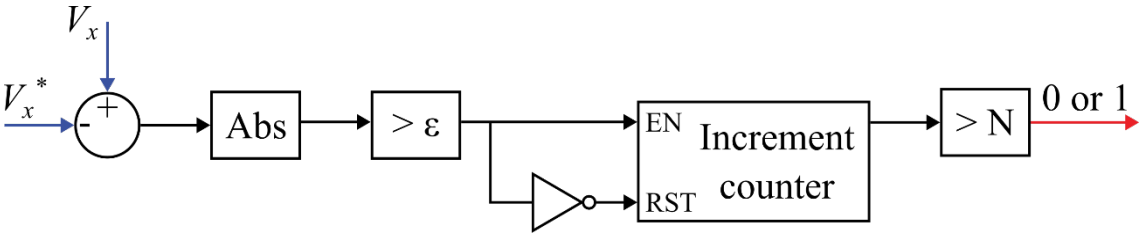

Figure 5.1 Schematic of the fault detection algorithm for output voltages

6 CONCLUSION

The deliverable focuses on the design of "Intelligent Power Modules with Integrated Sensors and OTP/OCP Circuits" within the RHODaS project. The main results of the deliverable can be summarized as follows:

- **Selection of Suitable SiC and GaN Devices:** Through rigorous testing and evaluation, appropriate SiC and GaN devices were identified for both converters, ensuring optimal performance and functionality. The report provides detailed information on the chosen GaN and SiC semiconductors for both low and high-power converters, highlighting their specific characteristics and suitability for the project. Table 6.1 summarises the selected semiconductors.

Table 6.1: Summary of the selected semiconductors.

Power converter	GaN	SiC
Low-power converter	GS66516T	G3R30MT12J
High-power converter	IGI60F017A1L	CAB450M12XM3

- **Functionalities and Driver Selection:** The required functionalities for the gate-driver circuit were defined, considering both in-house development and commercially available options. The chosen drivers for low and high-power converters were specified based on their compatibility with the desired functionalities. Table 6.2 shows the selected drivers.

Table 6.2: Summary of the selected drivers.

Power converter	Driver for GaN	Driver for SiC
Low-power converter	ADUM4121ARIZ	ADUM4135BRWZ
High-power converter	IGI60F017A1L	CGD12HBXMP

- **Sensor Integration:** The report outlines the selection and integration of sensors necessary for implementing the desired functionalities of the converter. Temperature, current and voltage sensors have been selected for high and low power converters. Table 6.3 summarises the chosen sensors.

Table 6.3: Summary of the selected sensors.

Sensor	Low-power converter	High-power converter
Temperature	NTCLE400E3103HA	NTC in the SiC module
Current	LA-25-NP	LF 306-S or LF505-S
Voltage	LV 25-P & DVC 1000-P	ACPL-C87BT-500E or ACPL-782T-300E

- **Fault Tolerance Analysis:** A comprehensive study was conducted to identify potential faults in semiconductors, including their causes and effects. An advanced fault detection algorithm, based on the integrated sensors and the drivers protections, was proposed to detect various semiconductor faults. Table 6.4 summarises the parameters to be monitored in the fault detection algorithm, as well as their fault condition and fault type.

Table 6.4: Summary of the fault detection algorithm.

Parameter to monitor	Fault condition	Fault type
Transistor temperatures	$\varepsilon < T_{cx}$	Transistor failure.
DC bus voltages	$\varepsilon < \lvert V_{DC} - (V_H + V_L) \rvert$	Failure in a capacitor, voltage sensor or transistor.
Output voltages	$\varepsilon < \lvert V_x^* - V_x \rvert$	Transistor failure.

Regarding any potential deviations from the DoA, no significant deviations were observed. The project remained on track, adhering to the planned activities and timelines. Contingency plans were considered during the selection of devices, drivers, and sensors, ensuring flexibility and adaptability to unforeseen challenges.

In summary, the report's findings highlight the successful design and implementation of power modules, offering valuable insights into the integration of sensors, selection of semiconductors, and fault tolerance analysis. These results contribute significantly to the overall progress and success of the RHODaS project.

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