D1.2. Materials specifications and requirements for active and passive electronic components. Selection matrix and integration strategies

Reinventing High-performance pOwer converters for heavy-Duty electric trAnSport

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DISCLAIMER

EXECUTIVE SUMMARY

This deliverable preselects the components for the active and passive parts of the power converter including sensors and interfaces.

Different GaN and SiC modules which fulfil the power requirements are compared. In the driver selection section protection features of GaN and SiC drivers are explained and available drivers are preselected.

The modules influence the size of the converter. Therefore, the deliverable includes an approximation of the final size of the converter considering the selected modules.

The IP rating required on some components is detailed. Considerations for thermal system components are also given.

As detailed in the project, the final material specifications and requirements for the electronic components will be set by month 15.

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1 SPECIFICATION OF ELECTRONIC COMPONENTS

This section specifies and lists the main components of the high-power hybrid T-type inverter. Table 1 summarizes the specifications of the inverter, which were previously defined in D1.1. Based on these specifications the main active and passive components were selected.

Table 1 High-power inverter specifications

Parameter	
Maximum efficiency	>98 %
DC bus voltage	1000 V
Rated power	150 kW
Maximum power	250 kW
Semiconductor	GaN + SiC
Topology	T-type (modular)
Switching frequency	50 – 100 kHz
Rated current	150 A
Maximum current (rms)	250 A

Figure 1 shows the main structure of the high-power Hybrid GaN-SiC T-type inverter which should be the main goal of project RHODAS as shown in the roadmap written in D1.1.

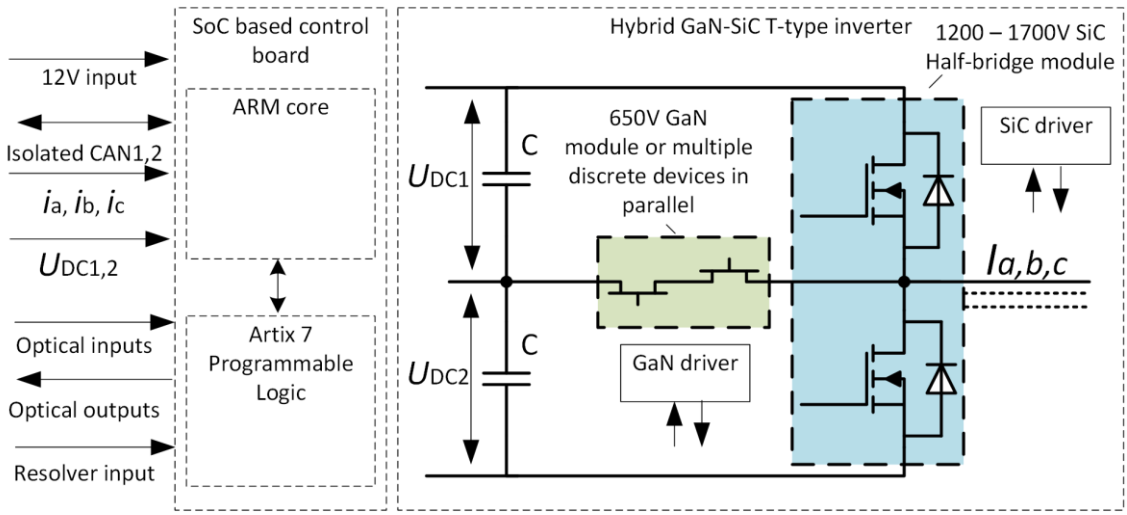


Figure 1 Structure of the high-power Hybrid T-type inverter

The inverter consists of a SoC (System on a Chip) based control board and the three-phase three-level hybrid inverter stage. The main advantage using such an SoC is the higher flexibility due to the included FPGA. The SoC includes an Artix 7 based FPGA which is responsible for generating the gate signals. The control board will provide two separate CAN bus interfaces as well as a resolver interface. The GaN and SiC driver are connected over optical interfaces to the control board.

1.1 GAN AND SIC SEMICONDUCTOR PRESELECTION

The converter designed in the RHODAS project is a 3-level T-type converter. Currently, there are no modules with this topology with SiC and GaN. Therefore, it is necessary to look for alternatives to build the converter.

Table 2 and Table 3 show available GaN and SiC devices and possible alternatives which are available on the market.

For the high currents required, SiC modules are preferred as opposed to discrete SiC devices. Most SiC modules are half-bridge modules. Therefore, the converter will use three separate half-bridge modules. In contrast to a 3-phase module, the half-bridge modules are intended to ensure that the design remains compact, and modular, with an additional T-type GaN branch and can be implemented with short DC link current paths.

The module from Wolfspeed (CAB450M12XM3) is currently available and meets the previous requirements. Additionally, it offers an easy way to mount the heatsink and is therefore the preferred SiC module.

Table 2 Preselected SiC semiconductors

Name and manufacturer	V_{ds} (V)	I_d (A)	$R_{ds(on)}$ (mΩ)	Configuration
MSCSM170AM039CT6AG / MICROCHIP	1700	416 (Tc = 80°C)	3.9 (@25°C) 6.8 (@175°C)	Half-bridge module
MSCSM120AM042CT6LIAG / MICROCHIP	1200	394 (Tc = 80°C)	4.2 (@25°C) 6.7 (@175°C)	Half-bridge module
NVVR26A120M1WSS / ONSEMI	1200	400	2.6(@25°C) 4.6 (@175°C)	Half-bridge module
CAB450M12XM3/ Wolfspeed	1200	450 (Tc = 25°C) 409 (Tc = 90°C)	2.6 (@25°C) 4.6 (@175°C)	Half-bridge module
CAB530M12BM3/ Wolfspeed	1200	719 (Tc = 25°C) 541 (Tc = 90°C)	2.7 (@25°C) 4 (@175°C)	Half-bridge module

Table 3 Preselected GaN semiconductors

Name and manufacturer	V_{ds} (V)	I_d (A)	$R_{ds(on)}$ (mΩ)	Configuration
GS66516T / GaN Systems	650	60 (@ 25°C) 47 (@100°C)	25 (@25°C) 65 (@150°C)	Single discrete semiconductor
GS-065-060-3-T / GaN Systems	650	60 (@ 25°C) 47 (@100°C)	25 (@25°C) 65 (@150°C)	Single discrete semiconductor
GS-065-060-5-T-A / GaN Systems	650	60 (@ 25°C) 41 (@100°C)	25 (@25°C) 65 (@150°C)	Single discrete semiconductor
GS-065-150-1-D2 / GaN Systems	650	150	10	Discrete die
Power Module / Amosense + GaN Systems	650	200 (Tc = 25°C)	-	Half-bridge module
Transfer Molded Power Device / Amosense + GaN Systems	650	100 (Tc = 25°C)	-	Half-bridge module

Table 3 shows that there is no common source module available which includes GaN semiconductors. Currently there are GaN modules from Amosense in development which offer a half-bridge configuration. They are not commercially available, and for a T-type inverter, two of such modules would be necessary to replace a common source module. However, GaN Systems is part of the project's industrial advisory board, and they may be able to supply these modules. Figure 2 shows the two Amosense GaN modules.

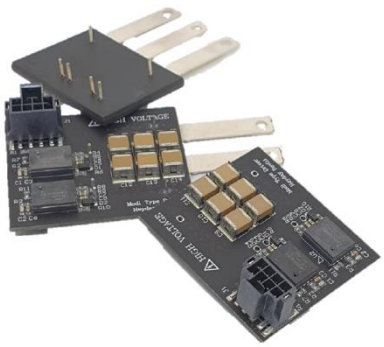
Power Module (Half-Bridge)	Transfer Molded Power Device (Half-Bridge)
	

Figure 2 Amosense GaN modules

An alternative approach is to use discrete GaN semiconductors which must be connected in parallel to handle the specified current. For example, using the pre-selected GS66516T from GaN Systems, at least 6 devices would have to be connected in parallel, which would be difficult to manage with a discrete setup.

If a high performance GaN module is not available, a maximum of two to three discrete GaNs are parallelized to mitigate the risks of the overall T-type topology, as GaN parallelization is a complex task. The current best option appears to be GaN Systems' GS-065-060-3-T, which is slightly improved over the GS66516T and thermally better than the GS-065-060-5-T-A.

If it were not possible to ensure the nominal power levels of the converter with the available GaN devices, a possible solution, already mentioned in D1.1, would be to switch the operation of the converter from three levels to two levels (that is, without intervention of the branch GaN), according to the power required by the load.

1.2 DRIVER SELECTION

Two different types of drivers are required to control the high-power hybrid inverter because SiCs and GaNs require different drive voltages, safety functions, and drive currents.

Drivers must have several protections and functionalities for the proper functioning of the converter. There are two main protections:

- **Crosstalk protection:** Drivers may have two drive inputs (V_I+ and V_I−) to control the gate of the transistor drive signals. With the V_I− pin low, the V_I+ pin accepts positive logic. If V_I+ is held high, the V_I− pin accepts negative logic. Table 4 shows a possible truth table of the drivers. Notice that the output is high only if V_I+ is high and VI- is low. Hence, both inputs are used to protect the transistor from noise, such as crosstalk. The procedure is the following: one input (V_I+) receives the PWM signal from the transistor itself. The other pin (V_I-) receives the PWM signal from the complementary transistor. Hence, the transistor will only activate when its signal is positive, and the complementary signal is negative. This method avoids false switching that can generate additional losses and even the destruction of the transistor. The same method may be applied using only a differential PWM signal.

Table 4 Desired truth table of the drivers

V_I-	**V_I+**	**V_{OUT} Output**
Don't care	Low	Low
Low	High	High
High	Don't care	Low

- **Miller clamp:** Drivers should have an internal Miller clamp to reduce voltage spikes on the gate. These spikes are caused by the Miller capacitance during the shutoff of the transistor. When the input gate signal requests the transistor to be turned off, the Miller clamp MOSFET is off initially. In most drivers, the clamp is activated at 2 V on the falling edge of the gate drive output. When the clamp is active, it creates a second low-impedance current path for the gate current to follow. The Miller clamp switch remains triggered until the input drive signal changes from low to high.

Some drivers present a series of additional protections to those mentioned above, such as:

- **Undervoltage lockout (UVLO):** Drivers have UVLO protections for the primary and secondary sides of the device. If either voltage is below the falling edge UVLO, the driver outputs a low signal, i.e. the transistor is turned off. The UVLO detection has some hysteresis for allowing small voltage source ripple.

- **Short circuits (saturation and overcurrent):** If saturation is detected, the driver shuts down the gate drive. Moreover, component failures may occur with the circuitry connected to the transistor connected to the driver, such as shorts in the motor windings or shorts to power buses. The resulting excess in current flow causes the semiconductor to come out of saturation. In this scenario, the driver enters the failure state and turns the transistor off.

- **Thermal shutdown:** the gate driver is disabled when the internal temperature of the driver exceeds a certain threshold. This state continues until the internal temperature drops.

The Gate driver for SiC module could be UCC5870-Q1 (TI Driver), or BM6112FV (Rohm Gate Driver), but many other options available on the market. The choice of the final gate driver depends heavily on the semiconductors selected, the isolation voltages, the required safety features, and the required drive currents. The gate charges of the semiconductor influence the required drive currents and thus the switching slope speeds and vary with the selected SiC and GaN.

For the GaNs isolated gate drivers with low UVLO voltages are required. Suitable drivers are Si8275GB-IS1, Si8275GBD-IS1, Si8275GB-IM1, Si8275GB-IM1, Si8271GB-IS, Si8271GBD-IS or ADUM4121ARIZ. The preferred GaN driver is the ADUM4121ARIZ because, unlike the others, it has a Miller clamp and will also be used in the low-power converter.

For driving the semiconductors isolated power supplies are necessary. Every switch will have its own isolated gate drive supply (no bootstrap circuit). Fitting DC/DC converters could be from Recom (RxxP2xxyy +15/-9 V), that are isolated, have enough power and provide necessary voltage levels. But a lot of other options are available on the market.

The GaNs require a gate drive of 6 V and therefore an isolated converter with this voltage will be used, of which there are many on the market, such as the NTE0506MC (1W) or the RP-0506S.

1.3 PASSIVE COMPONENTS

To minimize the commutation loop, Ceralink capacitors will be used in close proximity to the semiconductors such as the B58031U7504M062 or B58035U7105M052. They will keep parasitic inductances low and will deliver high currents. For higher capacitances, the DC link is supplemented with film capacitors.

The passive elements will be selected so that the circuit has a resonant frequency higher than the switching frequency. Additionally, the resonant frequency will not coincide with any switching harmonics.

1.4 SENSORS AND INTERFACES

The control PCB which includes a Xilinx Zynq XC7Z020-1CLG484C SoC will offer the following sensor and interface inputs:

Sensors:

- Current sensor front-end for: Closed loop Hall effect sensors like the LF 306-S or LF 505-S. These sensors offer high accuracy and bandwidth. The measurement range can be selected up to 500 A (peak).
- Two DC-link voltage measurement (V_{DC1} and V_{DC2}) inputs. DC voltage isolation sensor with integrated sigma-delta ADC (ACPL-C87BT-500E or ACPL-782T-300E) will be placed close to the DC-link bus bar to detect unbalance or overvoltage conditions.
- NTC or PT1000 temperature sensor inputs.

Interfaces:

- Minimum of 12 optical inputs (number of inputs and outputs must be defined) based on digital optical receiver 660nm (905EM660KM001/002).
- Minimum of 12 optical outputs based on Ratioplast Optical emitter 10Mbit/s 660nm (905SE660KM003) for 1mm plastic optical fiber.
- Two isolated CAN interfaces.
- One resolver interface based on the AD2S1200 (Excitation frequency and voltage: 10 kHz, ~7 V_{RMS}) resolver-to-digital converter.

2 SYSTEM INTEGRATION

This section gives some considerations on the integration of the converter in the IMD. In particular, it explains the design of the busbar, the selected connectors, the packaging, and the integration with the thermal system.

2.1 BUSBAR DESIGN

The first step in the busbar design process is to choose a suitable geometry for the semiconductors and the DC-link capacitors. The arrangement should be chosen in such a way that the power density is optimized and at the same time the busbar complexity is minimized. To achieve an equal current distribution the symmetry between DC-link capacitors and the SiC and GaN modules must be considered. In the next step proper terminal connections should be selected which are specified for the selected current [1]. The optimization of the busbar in terms of current density, inductance and temperature distribution will be done with the simulation tool Comsol Multiphysics [2].

2.2 CONNECTORS

The terminal connectors must be selected according to the inverter specifications summarized in Table 1. For the DC input Powerlok receptacles from Amphenol were preselected. Connectors from Fischer were selected for the low-voltage resolver and the CAN interface. Both connectors offer a high IP-class, as shown in Table 5.

Table 5 Preselected connectors

Name and manufacturer	Rated voltage / current	IP-class	Usage
PowerLok 300, 2 pole / Amphenol	1000V / 300Arms	67	DC input
PowerLok, 3 pole, 180 Degree Busbar Lug Receptacle / Amphenol	1000V / 300Arms	69k	AC output
Core-series, 6 pole / Fischer Connectors	50V / 60A	50 - 69	Resolver interface
Core-series / Fischer Connectors	50V / 60A	50 - 69	CAN interface and power supply

2.3 COMPONENTS IP CLASS

It is important to consider the IP degree of protection of different components, especially the engine and gearbox, which *Table 6 Components IP-class* show these degrees of protection.

Table 6 Components IP-class

Components	IP-class
EM	20
Gearbox	54

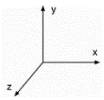
The electric machine is designed to be integrated in a gearbox housing. Since, the EM has to be tested in standalone with the power converters (T5.4), a housing needs to be designed for the EM. Consequently, the resulting IP class will be lower than expected.

2.4 PACKAGING

The packaging size is updated, based on new information regarding the GaN modules size. The following table and figures report the new estimations. A confirmation will be done in the second version of this deliverable in M15.

Table 7 Preliminary dimensions(1)

	X (length) (mm)	Y (height) (mm)	Z (width) (mm)
Overall powertrain	1790 max.	700 max.	600 max.(2)
Electric Motor	400 max.	380	380
Power Converter	400 max.	70 max.(3)	380 max.
Gearbox	590 max.	410 max.	595 max.
Differential	800 max.(4)	600 max.(4)	600 max.(4)

(1) Axis directions 

(2) Without the side shafts.

(2) Modified due to information on GaN modules.

(3) Based on conventional differential.

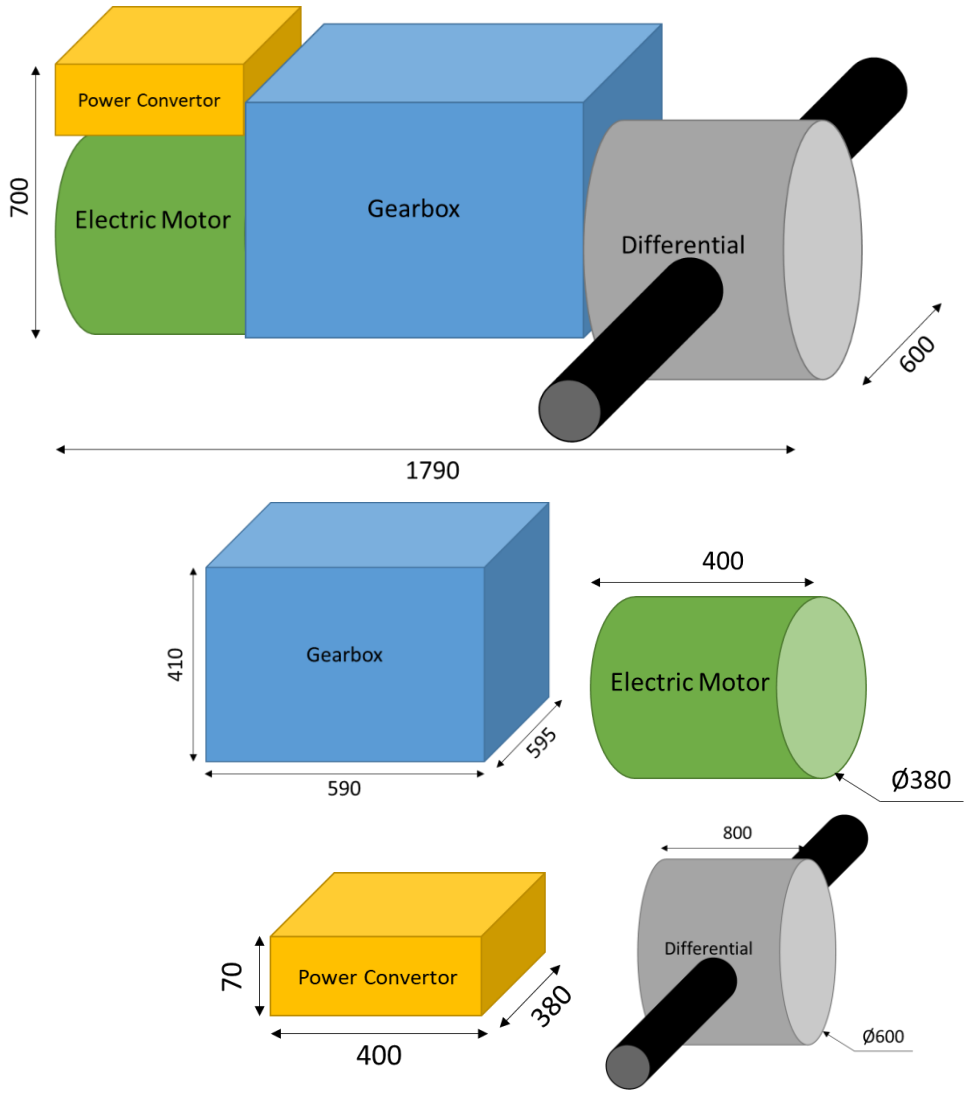


Figure 3 Preliminary dimensions of the IMD and its different parts

2.5 COOLERS

Thermal design is influenced by losses from the power components, which requires transport of thermal energy to a cooler ambient area. Since power transistors internally have a very small thermal intrinsic capacity, temperature at the core of a transistor may rise significantly if insufficient cooling is provided for the losses. In RHODAS the thermal design is delimited by the grant agreement and the component. The optimization of the cooler in terms of temperature distribution, thermal flux and fluid flow will be done with the simulation tool Comsol Multiphysics [2].

The specific size depends on the final design of the power electronics and the chosen housing. As a starting point Microchip / Microsemi MSCSM120AM042CT6LIAG is used for the number described regarding cooling materials.

Table 8: Thermal interface materials

Manufacturer	Name	Thickness (μm)	Thermal conductivity ($W/(m \cdot K)$)	Equivalent Thermal resistance ($\frac{mK}{W}$)
Panasonic Industrial devices and solutions	EYGS0610ZLAH Graphite Pad (compressible)	200	28	1.152
Dow	DOWSIL 340	60	0.67	14.444

Table 9: Glycol selection

Manufacturer	Name	Concentration	Minimum operating point
GLYKOL & SOLE GmbH	GLYKOSOL N	34%	-20 C
GLYKOL & SOLE GmbH	GLYKOSOL N	44%	-30 C

The interface material between power module can be either the graphite sheets or the thermal paste depending on the mechanical requirements. The thermal paste is a more flexible and cost-effective solution, but the graphite pads have superior performance.

The glycol may need consideration when used together with copper, depending on e.g., the concentration and free ions in the glycol [3]. The copper cold plate will be optimized based on the needed flow rate as a function of the losses generated by the inverter and the physical distribution of those losses.

3 CONCLUSION

This deliverable presents the material specifications and requirements for active and passive electronic components.

The deliverable presents the requirements for the electronic components and pre-selects some of them. Drivers, sensors, connectors, thermal interface materials and some passive elements are also pre-selected. The deliverable also pre-selects SiC and GaN transistors. For SiC transistors, the module CAB450M12XM3 is chosen due to its high-power density and low drain-source on-resistance ($R_{DS(ON)}$). The deliverable also compares various GaN semiconductors. However, there is no common source GaN modules available. Therefore, two options are possible:

- Using two half-bridge modules to form a T-type branch.
- Use discrete GaNs with reduced power for the 3-level operation.

The first option would drastically increase the size of the inverter and decrease the power density. The second option would limit the maximum current and therefore only allow 3-level operation in certain points as described in D1.1.

The dimensions of the power converter housing were adapted due to the size of the available power modules. These dimensions have been calculated considering the worst case from a volumetric point of view, i.e., assuming that the converter uses GaN half-bridge modules in antiparallel.

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[3] P. R. I. &. T. E. May, „The corrosion of copper in ethylene glycol-water mixtures containing chloride ions.,“ *Journal of Applied Electrochemistry - 21,* p. 358–364, 1991.